EE 5211
Analog Integrated Circuit Design

Hua Tang
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Today’s topic:

1. Introduction to Analog IC
2. IC Manufacturing (Chapter 2)
Introduction

• What is Integrated Circuit (IC) vs discrete circuits? Why?
The Transistor Revolution

First BJT transistor
Bell Labs, 1948
The First Integrated Circuit

Bipolar logic
1960’s

ECL 3-input Gate
Motorola 1966
Intel 4004 Micro-Processor

- 1971
- 1000 transistors
- < 1MHz operation
- 10μm technology
Intel Pentium (IV) microprocessor

2001
42 Million transistors
1.5 GHz operation
0.18μm technology
Intel Core™2 Duo Processor

2006
291 Million transistors
3 GHz operation
65nm technology
More recent

2007
>800 Million transistors
2 GHz operation
45nm technology (the biggest change in CMOS transistor technologies in 40 years)

2011 2nd-generation Core i7
1.2 Billion transistors
3.3 GHz operation
32nm technology
Introduction

• What is Analog Integrated Circuit (IC) vs Digital Integrated Circuit?
Analog versus Digital

• Information-bearing signals can be either analog or digital.

• Analog signal takes on a continuous range of amplitude values.

• Whereas digital signal takes on a finite set of discrete values (often binary) and frequently changes values only at uniformly spaced points in time

• Analog circuits:
  - circuits that connect to, create and manipulate arbitrary electrical signals
  - circuits that interface to the continuous-time “real” word
So why do we still need analog?

- The real world is analog (voice, light, heart-beat...)
- Many of the inputs and outputs of electronic systems are analog signal
- Many electronic systems, particularly those dealing with low signal amplitudes or very high frequency required analog approach

- *Lots of most challenging design problems are analog*

- *Good analog circuit designers are scarce* (very well compensated, gain lots of respect, regarded as “artists” because of the “creative” circuit design they do...)

Why A-D Interface?

- Nature is analog, not digital.
- A-D interface’s role is “translator”.

Analog World
- Twisted Pair Wires, Phone Lines
- MEMs Sensors, Actuators
- RF Electro-Magnetic Waves
- Microphones, Audio Devices

Digital World
- Storage Media
- Imagers, Display
The dominance of digital circuits actually increased the amount of analog electronics in existence. Nowdays, most electronic systems on a single chip contain both analog and digital (called Mixed-signal SoC (System on Chip)).

From Texas Instruments
Major Process Used in IC Fabrication

Microelectronics

Inert substrate
- Thick film
- Thin film

Active substrate
- Silicon
- GaAs

MOS
- NMOS
- PMOS
- CMOS

Bipolar
- TTL
- ECL
- Many linear ICs

MESFET

Bi-MOS
Basic semiconductor concepts

• A qualitative knowledge of semiconductor physics helps us understand the characteristics of diodes and other devices discussed later.

• Several materials are most often used for fabrication of solid-state electronic devices: silicon (Si), germanium (Ge) and gallium arsenide (GaAs)

• Silicon is most used, therefore a focus is put on Si in the discussion.
Intrinsic silicon

- Bohr model of an isolated silicon atom consists of a nucleus containing 14 protons.

- 14 electrons surround the nucleus in specific orbits (known as shells).

- The innermost shell (lowest energy) consists of 2 orbits. The next higher energy shell contains 8 orbits. The remaining 4 electrons occupy the outermost shell (called the valence shell).

- In intrinsic (pure) silicon, each atom takes up a lattice position having four neighbor atoms. Each pair of neighboring atoms forms a covalent bond consisting of two electrons orbiting the pair.

Figure 3.36 Intrinsic silicon crystal.
Intrinsic silicon II

• At absolute zero temperature, electrons take the lowest energy state available and all valence electrons are bound in covalent bounds and are not free to move. (silicon is an electrical insulator in this condition).

• However, in room temperatures (300K), a small fraction of the electrons gain sufficient thermal energy to break loose from the covalent bonds. These free electrons can easily move through the crystal.

• If voltage is applied to intrinsic silicon, current flows. However, the number of free electrons is small compared to a good conductor (so called semiconductor).

• Quantitatively, at room temperature only $1.45 \times 10^{10}$ free electrons per cm$^3$ among $5.0 \times 10^{22}$ atoms.

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**Figure 3.37** Thermal energy can break a bond, creating a vacancy and a free electron, both of which can move freely through the crystal.
**Intrinsic silicon III: conduction by holes**

- Free electrons are not the only means by which current flows in intrinsic silicon.

- Though it is the electrons that actually move, the vacancy or the hole can be thought of as a positive charge carrier that is free to move in the silicon. (bound electron can move only if a vacancy exists nearby).

- In an intrinsic silicon, an equal number of holes and free electrons are available, or $n_i = p_i$ where $n_i$ denotes the free electron concentration and $p_i$ hole concentration.

- When an electric field is applied to the intrinsic silicon, both types of carriers contribute to current flow.

*Figure 3.38* As electrons move to the left to fill a hole, the hole moves to the right.
N-type semiconductor

- Adding small amounts of suitable impurities to the crystal dramatically affects the relative concentration of holes and electrons. The resulting semiconductor is called extrinsic semiconductor.

- A material of impurity, such as phosphorus, have 5 valence electrons. It forms covalent bonds with their four neighbors and the 5th is only weakly bound to the atom.

- At certain temperature, the 5th electron can easily breaks its bond with the atom and becomes a free electron. However, a hole is not created by the impurity atom as the positive charge that balances the free electron is locked in the ionic core of the atom (or no covalent bond vacancy)

- Impurities that does this is known as donors to silicon and the resulting material is called N-type semiconductor material.

- In N-type material, conduction is mainly due to free electrons. Thus free electrons are called majority carriers and holes called minority carriers.

- Donor atoms giving up their 5th electron is said to become ionized. Positive charge is associated with each ionized atom.

- Net charge concentration is zero, ie. positive charge of ionized donors and holes is equal to negative charge of electrons.
Figure 3.39  *n*-type silicon is created by adding valence five impurity atoms.
P-type semiconductor

• In contrast to N-type semiconductor, impurity such as boron can be added to intrinsic silicon to form P-type semiconductor.

• Each impurity atom forms covalent bonds with three of its neighbors, but it does not have the 4th electron to complete the bond with the 4th neighbor.

• At usual operating temperatures, an electron from a nearby silicon atom moves in to fill the fourth bond of each impurity atom. This creates a hole moving freely through the crystal.

• Since the electron is bound to the ionized impurity atom, conduction in P-type material is mainly due to holes. Holes are called majority carriers and electrons minority carriers.

• The impurities are called acceptors because they accept an extra electron.

• Ionized impurity atom has negative charge. The concentration of holes is equal to the sum of concentration of free electrons and that of acceptor atoms.
Figure 3.40  $p$-type silicon is created by adding valence three impurity atoms.
Basic IC circuit component: MOS transistor

MOS: Metal Oxide Semiconductor
Modern dual-well CMOS Process

Dual-Well Trench-Isolated CMOS Process
CMOS Process at a Glance

1. Define active areas
2. Etch and fill trenches
3. Implant well regions
4. Deposit and pattern polysilicon layer
5. Implant source and drain regions and substrate contacts
6. Create contact and via windows
7. Deposit and pattern metal layers
CMOS Process Walk-Through

(a) Base material: p+ substrate with p-epi layer

(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

(c) After plasma etch of insulating trenches using the inverse of the active area mask
CMOS Process Walk-Through

(d) After trench filling, CMP planarization, and removal of sacrificial nitride

(e) After n-well and $V_{Tp}$ adjust implants

(f) After p-well and $V_{Tn}$ adjust implants
CMOS Process Walk-Through

(g) After polysilicon deposition and etch

(h) After n+ source/drain and p+ source/drain implants. These steps also dope the polysilicon.

(i) After deposition of SiO insulator and contact hole etch.
CMOS Process Walk-Through

(j) After deposition and patterning of first Al layer.

(k) After deposition of SiO insulator, etching of via’s, deposition and patterning of second layer of Al.
Advanced Metallization
Design Rules
Design Rules

• Interface between designer and process engineer

• Guidelines for constructing process masks

• Unit dimension: Minimum length
  – scalable design rules: lambda parameter (SCMOS SUBMICRON Design Rules)
  Technology=2 lambda
  – absolute dimensions (micron rules)
Layers in 0.25 μm CMOS process

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal</td>
<td>m1, m2, m3, m4, m5</td>
</tr>
<tr>
<td>well</td>
<td>nw</td>
</tr>
<tr>
<td>polysilicon</td>
<td>poly</td>
</tr>
<tr>
<td>contacts &amp; vias</td>
<td>ct, v12, v23, v34, v45</td>
</tr>
<tr>
<td>active area and FETs</td>
<td>ndif, pdif, nfct, pfct</td>
</tr>
</tbody>
</table>
Intra-Layer Design Rules

- **Well**
  - Same Potential: 0 or 6
  - Different Potential: 9

- **Active**
  - 3

- **Select**
  - 2

- **Polysilicon**
  - 2

- **Contact or Via**
  - 3

- **Metal1**
  - 2
  - 3

- **Metal2**
  - 4
  - 3
Vias and Contacts

Metal to Poly Contact

Metal to Active Contact

Via
CMOS Inverter Layout

(a) Layout

(b) Cross-Section along A-A’
Design Rule Check

poly_not_fet to all_diff minimum spacing = 0.14 um.
Feature size

The minimum feature size a CMOS process is roughly the minimum allowable value for L and W. For example, in a 5um process the minimum permissible value of L and W would be 5um.

Feature size keeps scaling down in the past years, eg. 2um, 1um, 0.5um, 0.35um, 0.25um, 0.18um, 0.13um, 90nm, 65nm, 45nm, 33nm, 23nm, ...