Today's topic:

1. Basic current mirrors
2. single-stage amplifiers
3. differential amplifiers

Chapter 3

The purpose of this Chapter is to discuss fundamental circuit building blocks.

A good knowledge of these basic building blocks is critical to understanding many subjects to be discussed later.

CMOS current mirrors and gain stages are emphasized here, while the general small-signal analysis method can be applied to BJT versions.

When analyzing transistor circuits to determine their small-signal behavior, it is implicitly assumed that signals are small enough that linear approximations about an operating point (Q point) accurately reflect how the circuit operates. These linear approximations may be represented schematically by replacing transistors with small-signal equivalent circuit, whose parameters (such as g_m, r_{ds} etc) are determined from the operating point.

A note on notations in the book and the lecture:

To the extent possible in this chapter, operating point quantities are represented with uppercase voltage and current symbols (e.g., V_{GS}, I_D) and small-signal quantities with lowercase symbols (e.g., v_{gs}, i_d). However, the practicing designer must always be alert to imprecise notation and remain able to interpret meanings within their proper context.

A general procedure for small-signal analysis:

a. Set all signal sources to zero and perform an operating point analysis for all currents and voltages. A voltage source set to 0 V is the same as an ideal wire—a short circuit. A current source set to 0 A is the same as an open circuit.

b. Replace all transistors with their small-signal equivalents where the parameters g_m, r_{ds}, etc, are found from the operating point voltages and currents using the relationships in summarized in Section 1.3.

c. Set all independent sources equal to zero, except for the signal sources that were zeroed in step (a). This includes power supply voltages, bias currents, etc. Remember that setting a voltage source to zero means replacing it with a short circuit, and setting a current source to zero means replacing it with an open circuit.

d. Analyze the resulting linearized small-signal circuit to find small-signal node voltages, branch currents, small-signal resistances, etc.

e. If desired, the complete solution may be found by superimposing the results of the operating point analysis in step (a) and those of small-signal analysis in step (d). The result so obtained is approximate because the small-signal analysis approximates transistor nonlinear behavior with linearized models.

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3.1 A simple current mirror

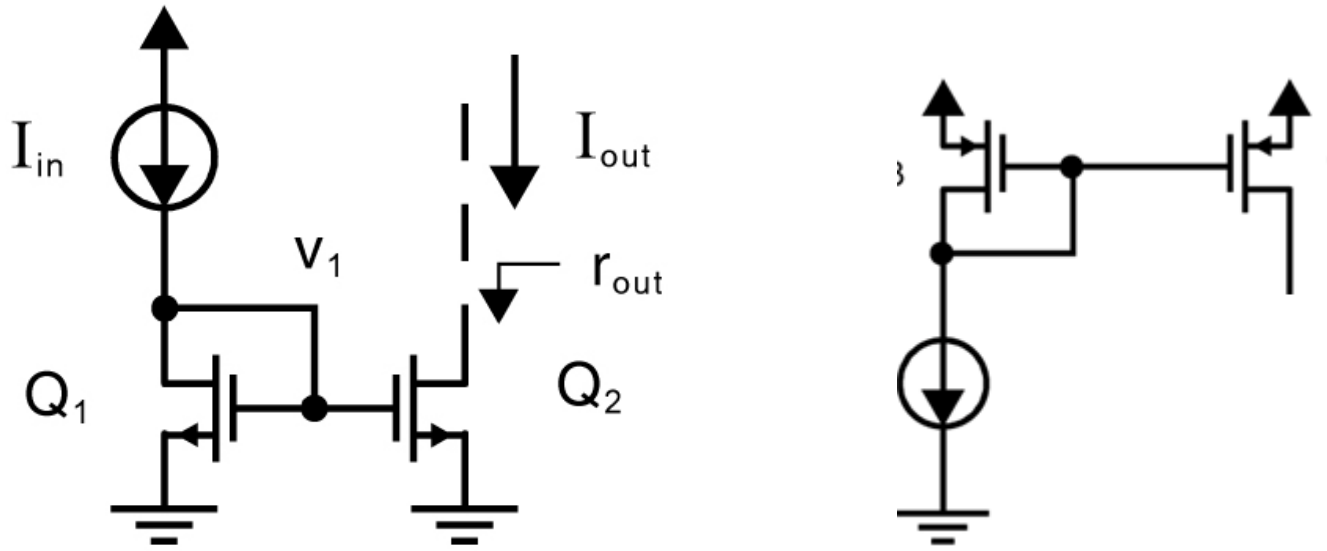
An ideal current mirror is a two port circuit that accepts an input current I_{in} and produce an output current $I_{out}=I_{in}$.

Also, an ideal current mirror will have zero input resistance but high output resistance.

Both transistors are in active region (so the drain voltage of Q2 must be larger than V_{eff2}).

If Q1 and Q2 have the same size, and finite r_{ds} is ignored, then Q1 and Q2 have the same current (due to the same V_{gs})

However, when r_{ds} are considered, the transistor with larger V_{ds} will have larger current.



Chapter 3 Figure 01

A simple current mirror: input resistance

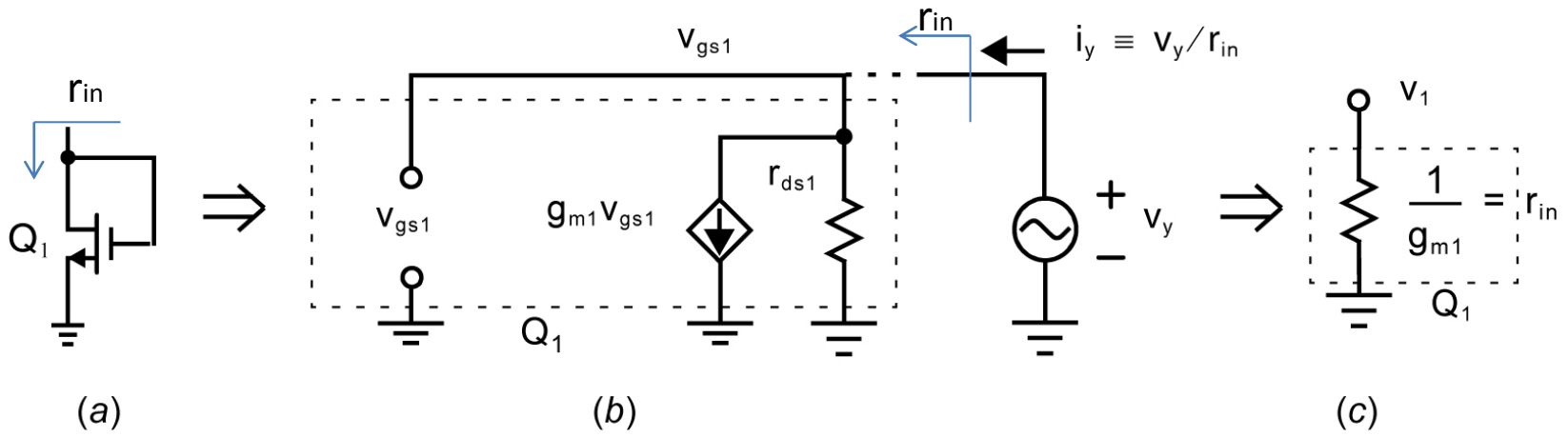
We can use the following small-signal equivalent circuit to compute the input resistance of the current mirror. (I_{in} is open and low-frequency model is used).

Then, apply a test signal voltage V_y at node V_1 and measure the current i_y

$$i_y = \frac{v_y}{r_{ds1}} + g_{m1} v_{gs1} = \frac{v_y}{r_{ds1}} + g_{m1} v_y$$

Input resistance is given by $r_{in} = V_y/i_y = 1/g_{m1} \| r_{ds1} \cong 1/g_{m1}$

Q1 is sometimes referred to as a diode-connected transistor.

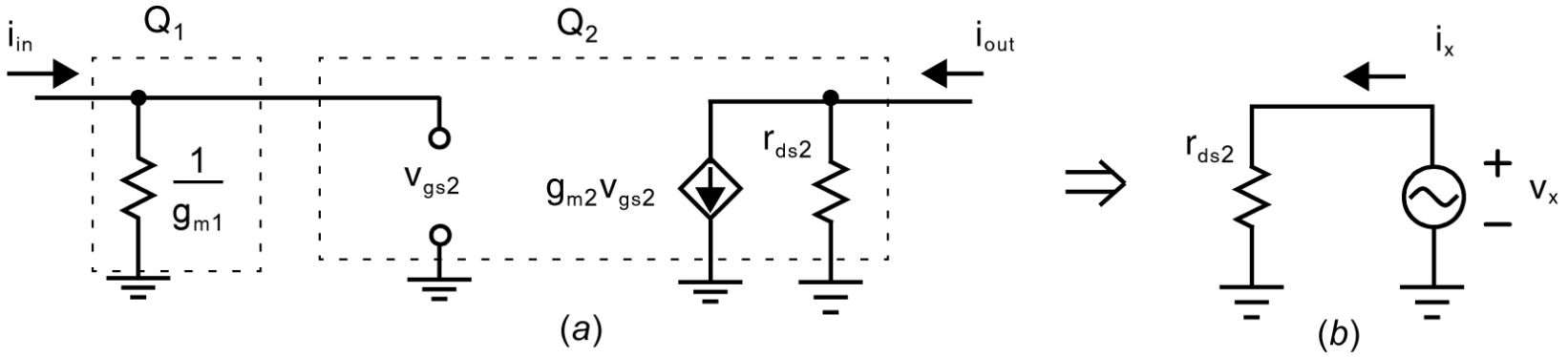


Chapter 3 Figure 02

A simple current mirror: output resistance

Using the model for the input resistance from previous slides leads to a simplified small-signal equivalent circuit for the overall current mirror. .

Output resistance is given by $r_{out}=V_x/i_x = r_{ds2}$



Chapter 3 Figure 03

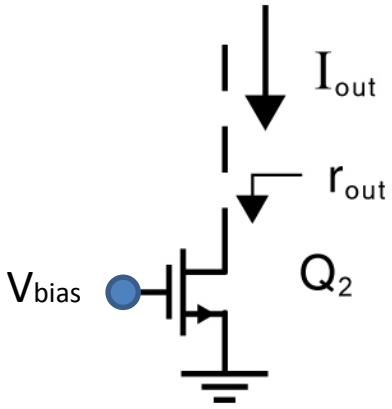


Figure 01

$r_{out} = r_{ds2}$

In this configuration, as long as gate terminal is small-signal ground, the resistance looking into the drain is r_{ds2}

A simple current mirror: output resistance

Using the model for the input resistance from previous slides leads to a simplified small-signal equivalent circuit for the overall current mirror. .

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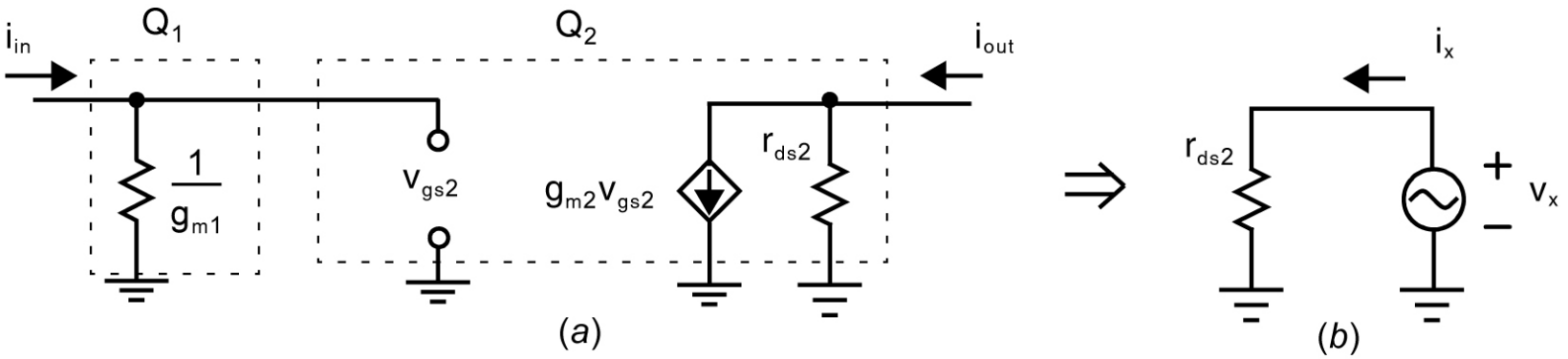


Chapter 3 Figure 03

An example 3.1 (page 119)

Consider the current mirror shown in Fig. 3.1, where $I_{in} = 100\ \mu A$ and each transistor has $W/L = 10\ \mu m/0.4\ \mu m$. Given the 0.35-μm CMOS device parameters in Table 1.5, find r_{out} for the current mirror and the value of g_{m1}. Also, estimate the change in I_{out} for a 100 mV change in the output voltage. What voltage must be maintained at the drain of Q_2 to ensure it remains in active mode?

$$r_{out} = r_{ds2} = \frac{L}{\lambda L I_D} = \frac{0.4\ \mu m}{(0.16\ \mu m/V)(100\ \mu A)} = 25\ k\Omega$$

$$g_{m1} = \sqrt{2\mu_n C_{ox}(W/L)I_{D1}} = 0.97\ mA/V$$

$$r_{s1} = 1/g_{m1} \cong 1.03\ k\Omega.$$

$$\Delta I_{out} = \frac{\Delta V}{r_{out}} = \frac{100\ mV}{25\ k\Omega} = 4\ \mu A$$

Estimation using low-frequency small-signal linear equivalent circuit

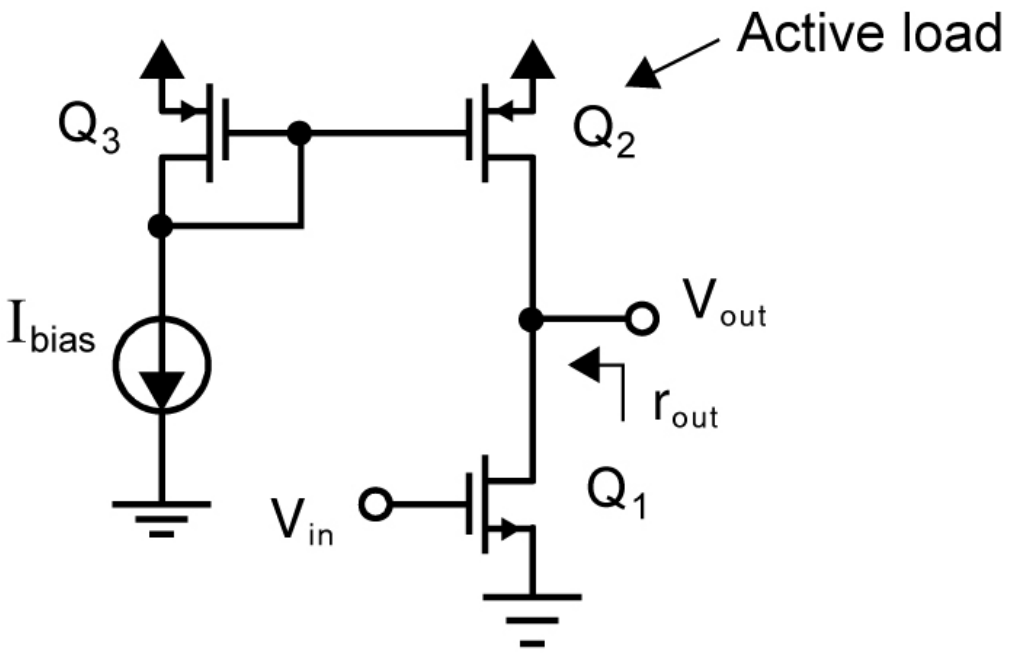
$$V_{eff2} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}} = 205\ mV$$

3.2 A common-source amplifier

A common use of simple current mirrors is to be active loads in a single-stage amplifier.

By using an active load, a high-impedance output load can be realized without using excessively large resistors or a large power supply voltage (for example, a 100k resistor load with 100µA bias current would need a power supply of at least 10V).

The common-source (CS) topology is the most popular gain stage, especially when high input impedance is desired.



Chapter 3 Figure 04

Small-signal analysis of CS: DC gain Av

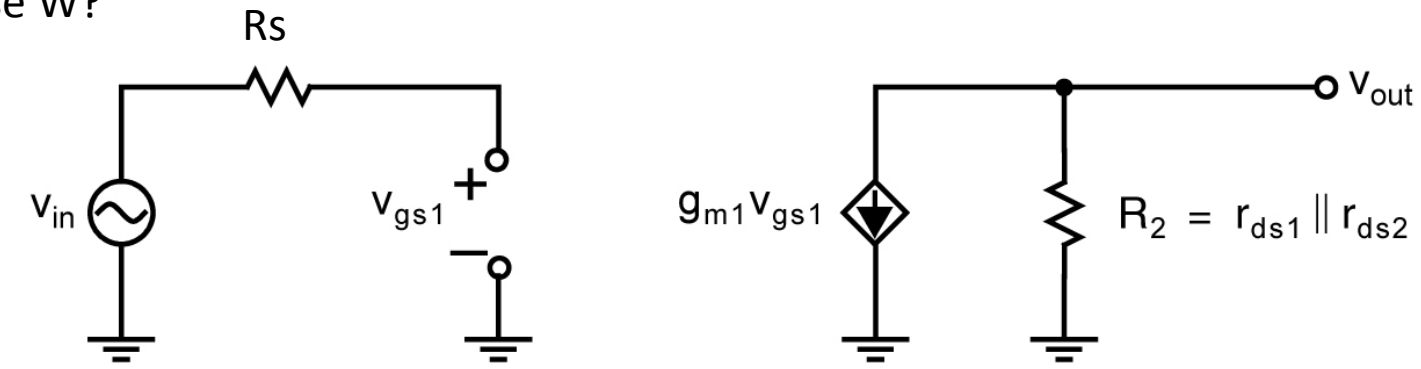
Assume that all transistors are in active region, the small-signal model of the CS amplifier with active load is shown below:
(note the resistance R2 is made up of parallel of r_{ds1} and r_{ds2}.)

$$A_V = \frac{v_{out}}{v_{in}} = -g_{m1}R_2 = -g_{m1}(r_{ds1} \parallel r_{ds2})$$

Depending on device sizes, currents and technology used, the typical gain for a CS amplifier could be between -5 to -100.

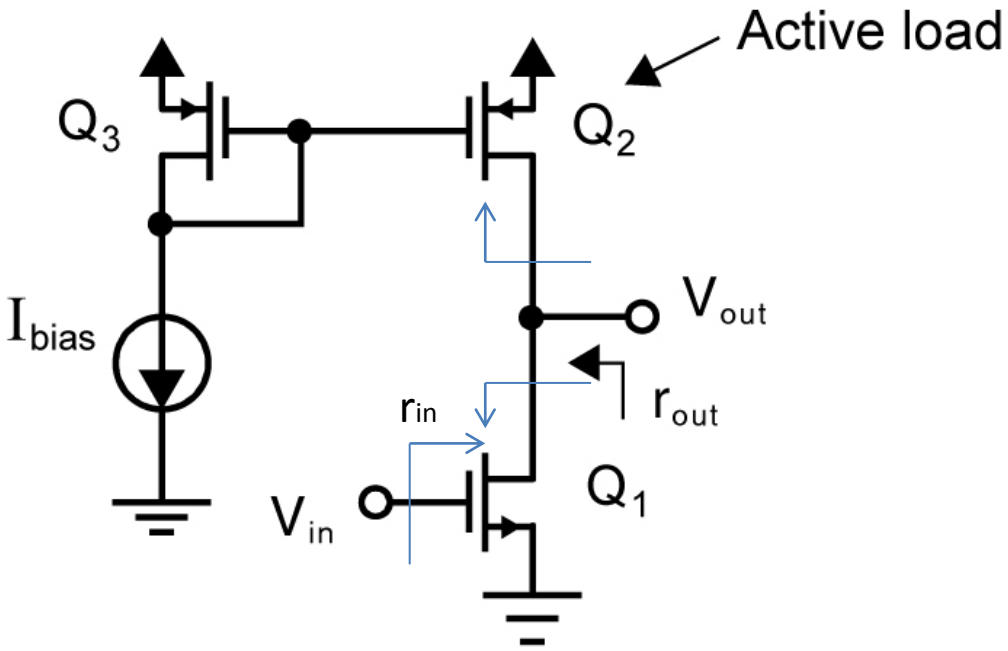
A_v is about one half of the intrinsic gain of Q1: $A_i = g_{m1}r_{ds1} \approx 2/(\lambda V_{eff})$. if $r_{ds2} \approx r_{ds1}$

To maximize the gain, it is desirable to minimize V_{eff1}. For a fixed bias current, this is to increase W?

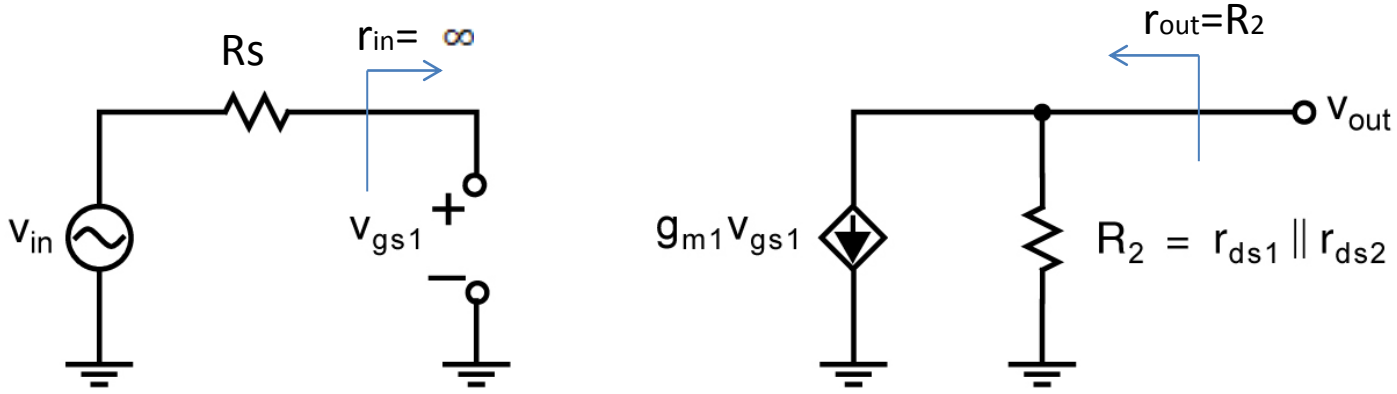


Chapter 3 Figure 05

Small-signal analysis of CS: r_{in} and r_{out}



Chapter 3 Figure 04



Chapter 3 Figure 05

An example 3.2 and 3.3 (page 121)

Assume $I_{bias} = 100\ \mu A$, all transistors have $W/L = 10\ \mu m/0.4\ \mu m$ in Fig. 3.4, and the device parameters are those of the 0.35-μm CMOS process in Table 1.5. What is the gain of the stage?

$$g_{m1} = \sqrt{2\mu_n C_{ox}(W/L)_1 I_{bias}} = 0.97\ mA/V$$

$$r_{ds1} = r_{ds2} = \frac{L}{\lambda L I_D} = \frac{0.4\ \mu m}{(0.16\ \mu m/V)(100\ \mu A)} = 25\ k\Omega$$

$$A_V = -g_{m1}(r_{ds1} \parallel r_{ds2}) = -0.97\ mA/V(25\ k\Omega \parallel 25\ k\Omega) = -12.1\ V/V$$

Modify the design in Example 3.2 to increase the gain by 20% by changing only the device width, W.

Neglecting higher-order effects, with the drain current fixed the output resistance ($r_{ds1} \parallel r_{ds2}$) is nominally unchanged. Hence, in order to increase gain by 20%, we must increase g_{m1} by 20%. Due to the square-root dependence of g_m on W (with fixed current), this in turn requires a 44% increase in W_1. Hence, the new size of Q_1 is (14.4 μm/0.4 μm). The resulting gain is

$$g_{m1} = \sqrt{2\mu_n C_{ox}(W/L)_1 I_{bias}} = 1.17\ mA/V$$

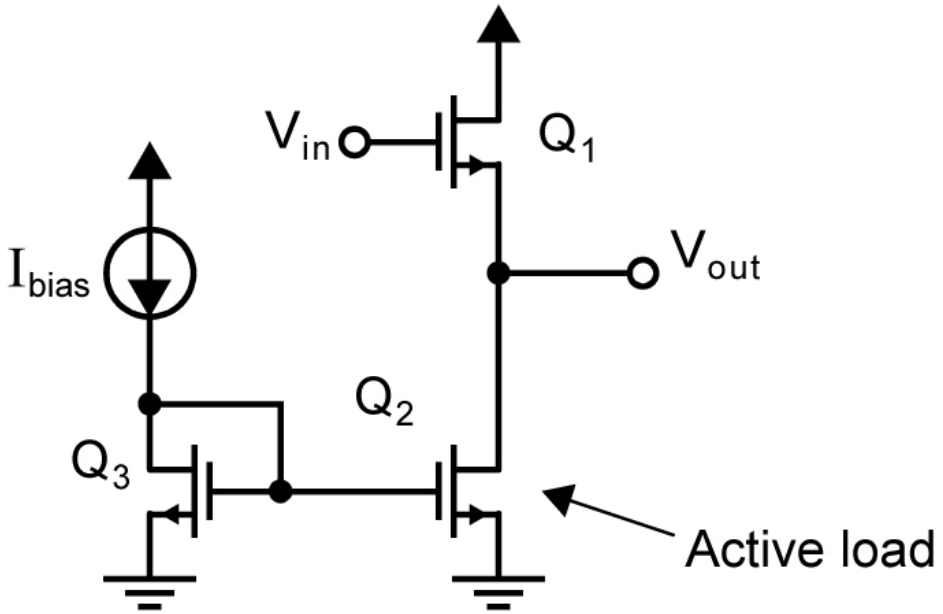
$$\Rightarrow A_V = -g_{m1}(r_{ds1} \parallel r_{ds2}) = -1.17\ mA/V(25\ k\Omega \parallel 25\ k\Omega) = -14.6\ V/V$$

$$V_{eff1} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}} = 171\ mV$$

3.3 A common-drain amplifier

Another general use of current mirrors is to supply the bias current for a common-drain or source follower (SF) amplifier.

SF amplifiers are commonly used as voltage buffers.



Chapter 3 Figure 06

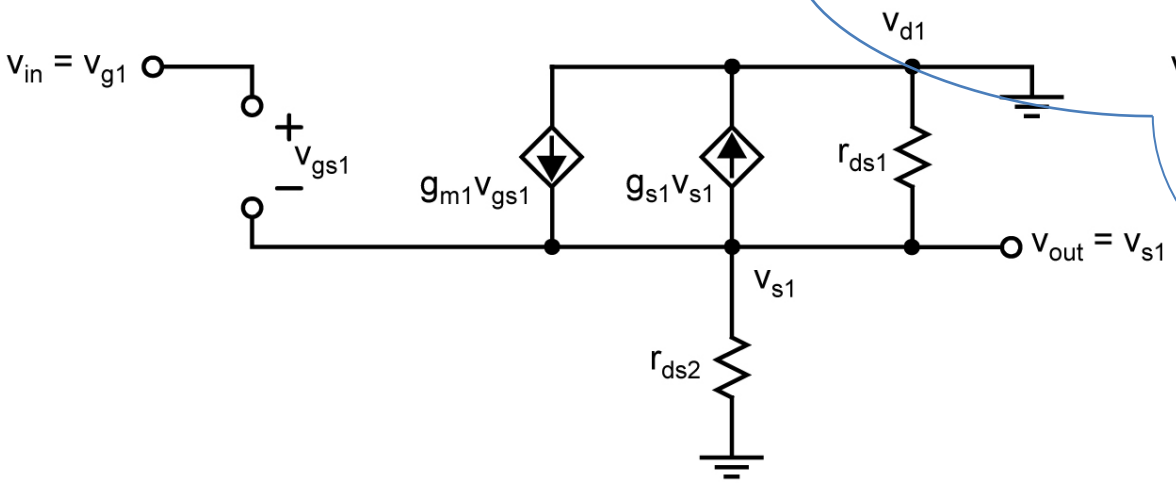
Small-signal analysis of SF amplifier: gain Av

In the small-signal model, note that the voltage-controlled current source that models the body effect of MOS transistors is included as there is finite source-body voltage (unlike CS amplifier), which may become a major limitation on the small-signal gain.

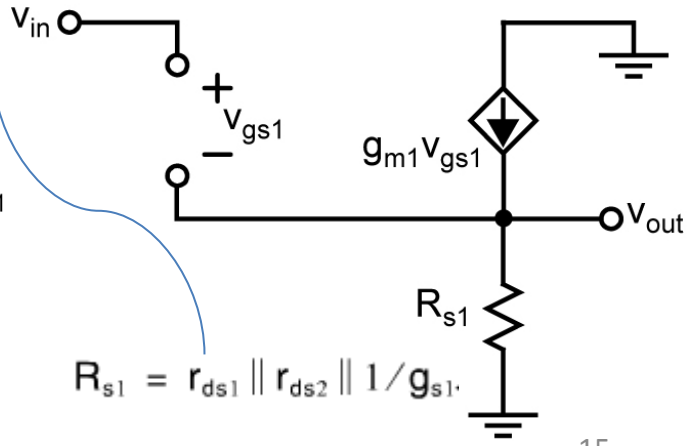
Note that the voltage-controlled current source modeling the body effect produces a current that is proportional to the voltage across it, which makes it equivalent to a resistor of $1/g_{s1}$. This allows to simplify the circuit to the right-hand side.

$$v_{out}/R_{s1} - g_{m1}(v_{in} - v_{out}) = 0$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + G_{s1}} = \frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}} = g_{m1}\left(\frac{1}{g_{m1}} \| \frac{1}{g_{s1}} \| r_{ds1} \| r_{ds2}\right)$$

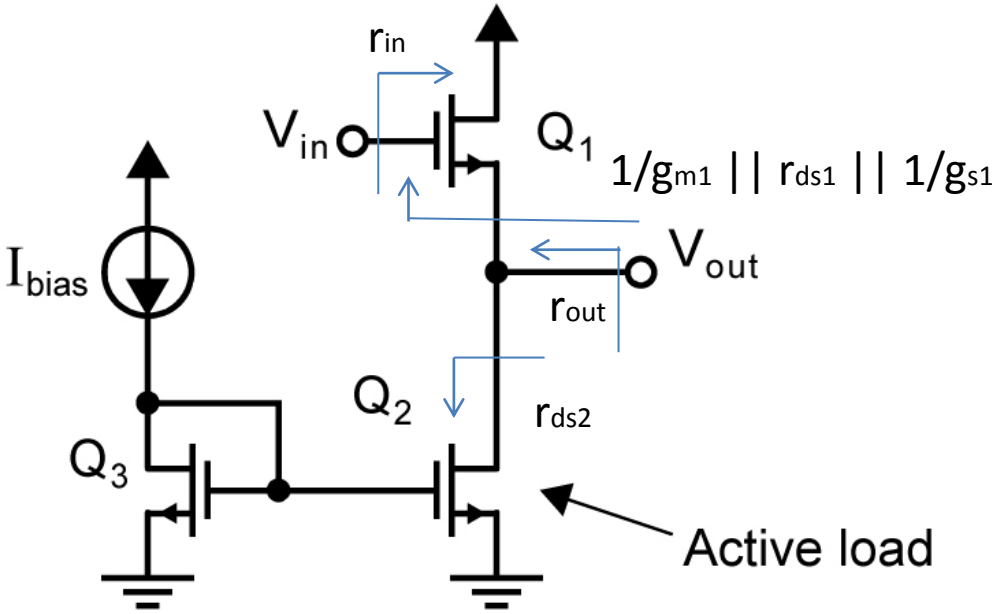


Chapter 3 Figure 07

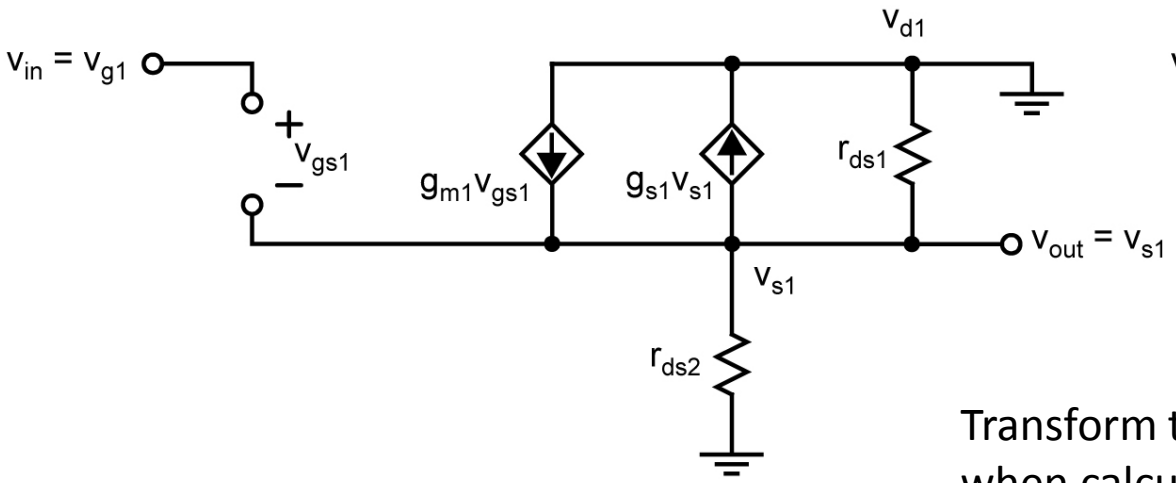


Chapter 3 Figure 08

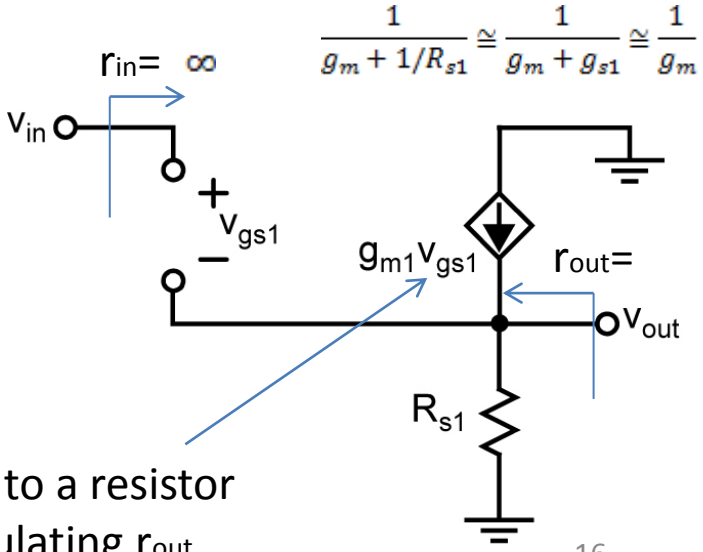
Small-signal analysis of SF: r_{in} and r_{out}



Chapter 3 Figure 06



Chapter 3 Figure 07



$$\frac{1}{g_m + 1/R_{s1}} \cong \frac{1}{g_m + g_{s1}} \cong \frac{1}{g_m}$$

Transform to a resistor when calculating r_{out}

Chapter 3 Figure 08

Example 3.4 (page 123)

Consider the source follower of Fig. 3.6 where $I_{bias} = 100\ \mu A$, all transistors have $W/L = 2\ \mu m/0.2\ \mu m$, $\phi_F \cong 0.4$ V and $\gamma = 0.3\ V^{-1/2}$, and the other device parameters are those of the 0.18-μm CMOS process in Table 1.5. What is the gain of the stage? assume that $V_{SB} \approx 0.5$ V

$$g_{m1} = \sqrt{2\mu_n C_{ox}(W/L)_1 I_{bias}} = 0.735\ \text{mA/V}$$

$$r_{ds1} = r_{ds2} = \frac{L}{\lambda L I_D} = \frac{0.2\ \mu m}{(0.08\ \mu m/V)(100\ \mu A)} = 25\ k\Omega$$

$$g_{s1} = \frac{\gamma g_m}{2\sqrt{V_{SB} + |2\phi_F|}}$$

$$g_{s1} = \frac{0.3\ V^{-1/2} \cdot g_m}{2\sqrt{0.5\ V + 0.8\ V}} \cong 0.13 g_m = 0.1\ \text{mA/V}$$

$$A_V = \frac{0.735\ \text{mA/V}}{0.735\ \text{mA/V} + 0.1\ \text{mA/V} + 0.04\ \text{mA/V} + 0.04\ \text{mA/V}} = 0.8\ \text{V/V} = -1.9\ \text{dB}$$

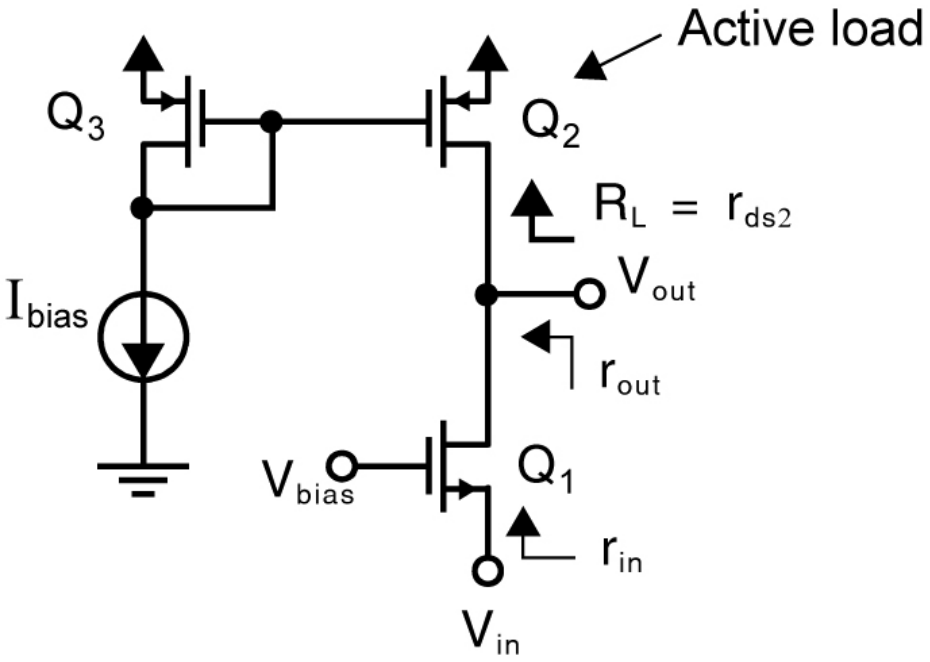
	0.18 μm	
	NMOS	**PMOS**
	270	70
	0.45	–0.45
	0.08	0.08
	8.5	8.5
	5	5
	1.6	1.7
	1.7	1.0
	1.6	2.4
	0.35	0.35
	0.50	0.55

Hence, it can be seen that body-effect is the major source of error causing the gain of the SF amplifier to be less than 1.0.

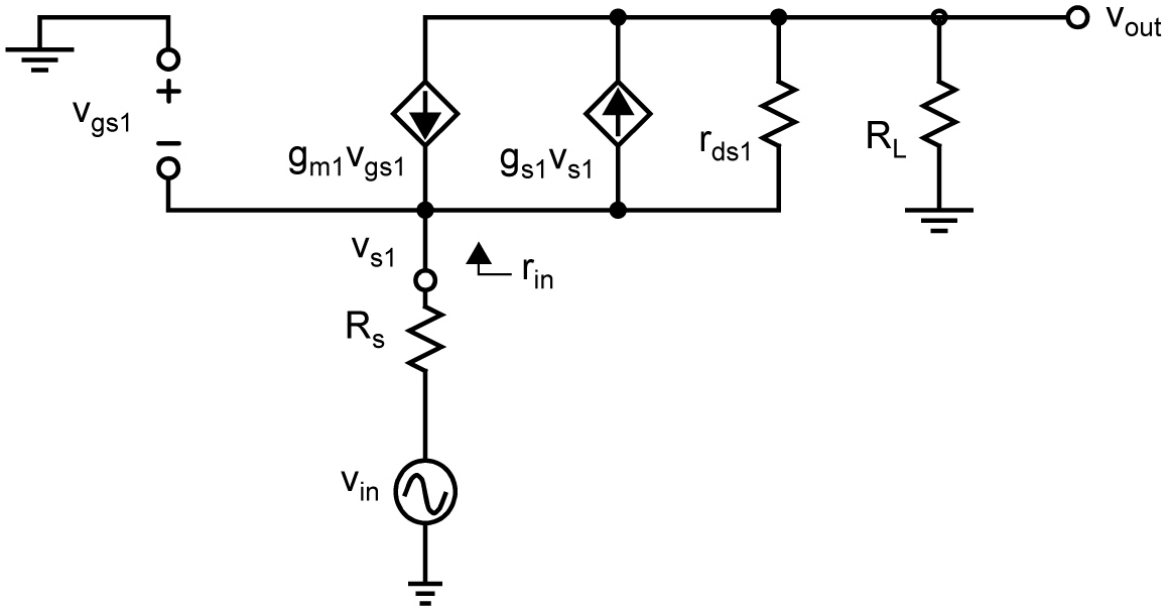
3.4 A common-gate amplifier

A common-gate amplifier is used as a gain stage when small input impedance is desired. Also, it is often used when the input signal is a current as small input impedance is desired.

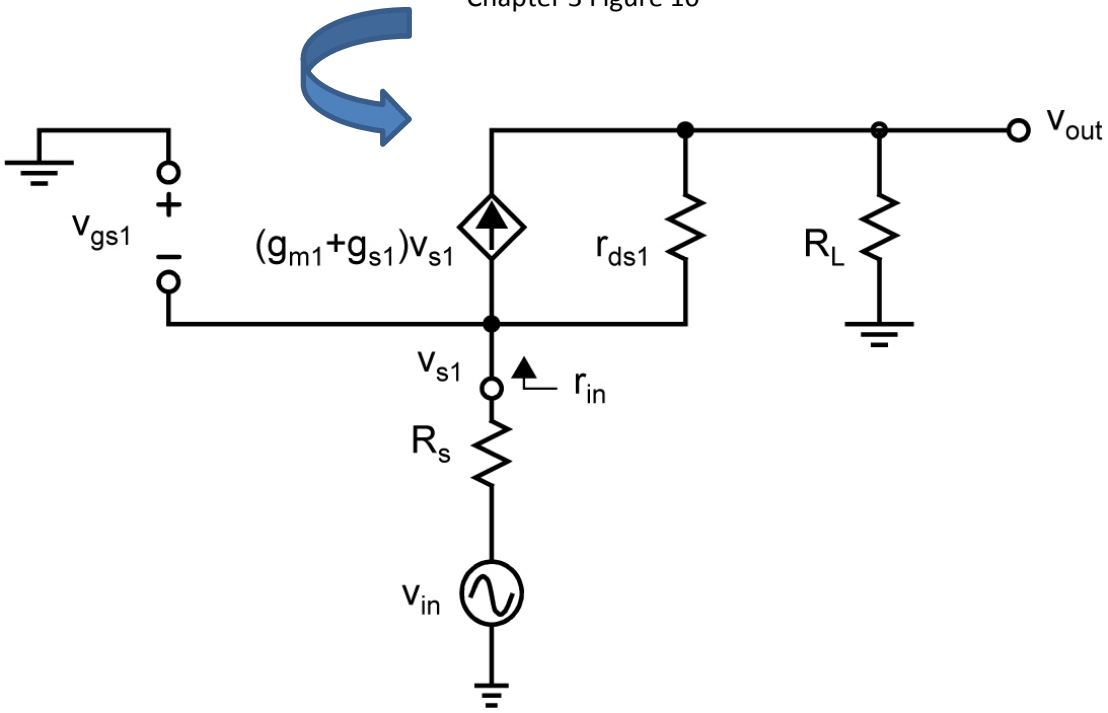
Aside from its low input impedance, the common-gate amplifier is similar to a CS amplifier as the input signal is across Gate-Source terminal and output taken from the Drain terminal. Hence, in both amplifiers, the small signal gain equals the product of g_m and total impedance at the drain.



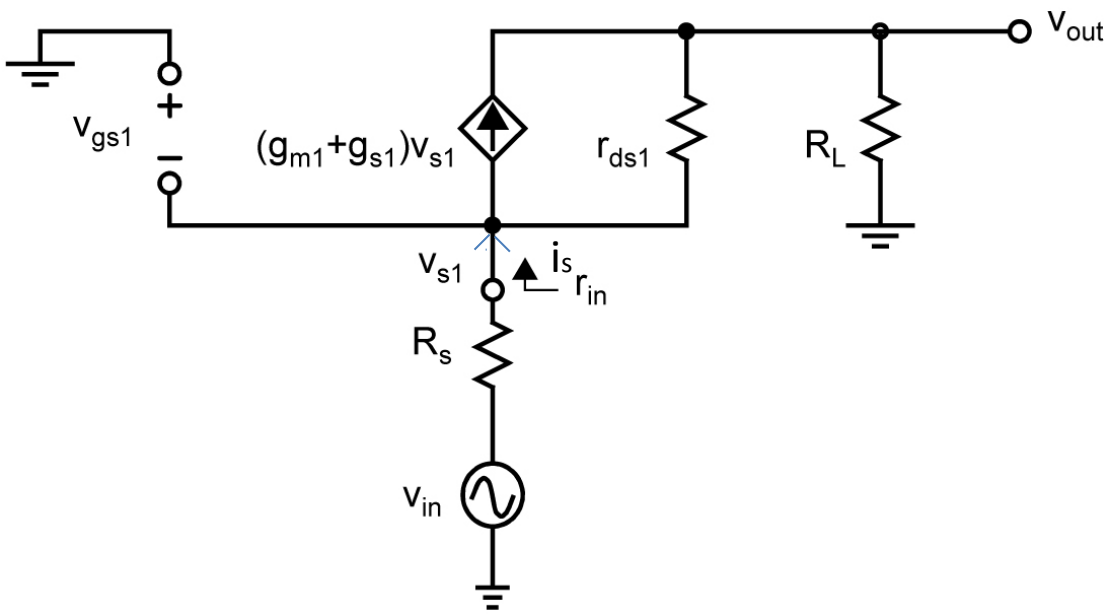
Chapter 3 Figure 09



Chapter 3 Figure 10



Chapter 3 Figure 11



Chapter 3 Figure 11

$$v_{out}(G_L + g_{ds1}) - v_{s1}g_{ds1} - (g_{m1} + g_{s1})v_{s1} = 0$$

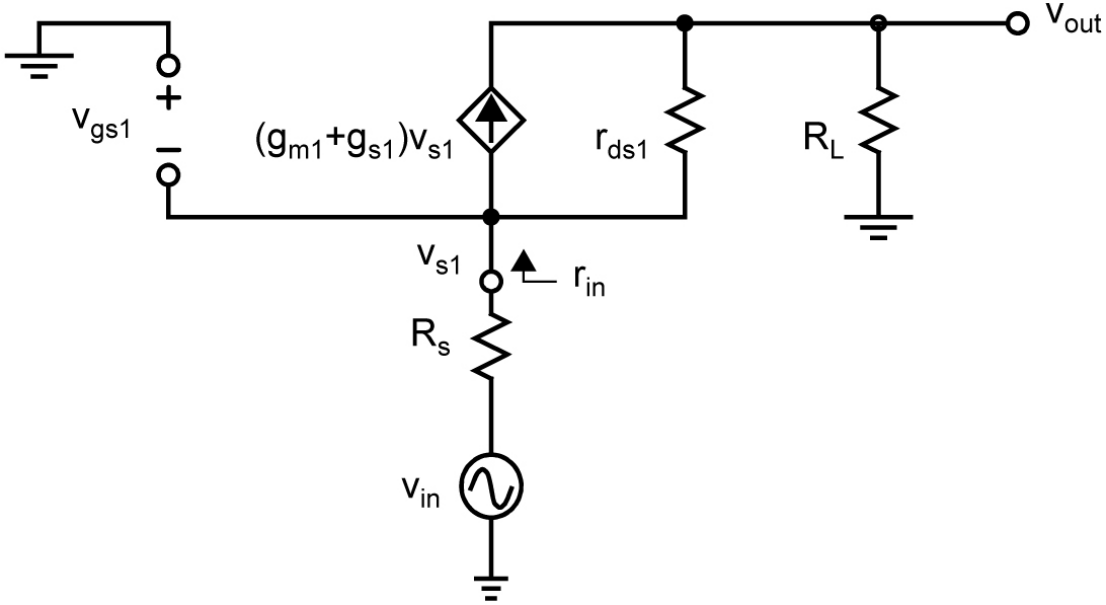
$$\Rightarrow \quad \frac{v_{out}}{v_{s1}} = \frac{g_{m1} + g_{s1} + g_{ds1}}{G_L + g_{ds1}} = (g_{m1} + g_{s1} + g_{ds1})(R_L \parallel r_{ds1}) \cong g_{m1}(R_L \parallel r_{ds1})$$

$$i_s = v_{s1}(g_{m1} + g_{s1} + g_{ds1}) - v_{out}g_{ds1}$$

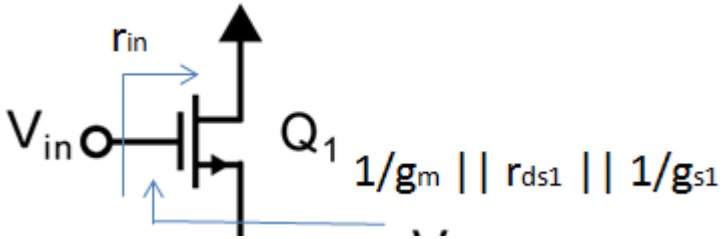
$$\Rightarrow \quad g_{in} \equiv \frac{i_s}{v_{s1}} \equiv \frac{g_{m1} + g_{s1} + g_{ds1}}{1 + \dfrac{g_{ds1}}{G_L}}$$

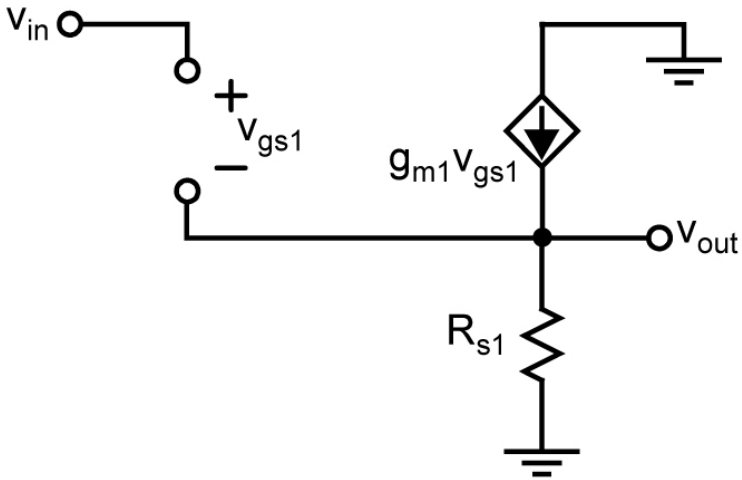
$$r_{in} = \frac{1}{g_{in}} = \left(\frac{1}{g_{m1}} \parallel \frac{1}{g_{s1}} \parallel r_{ds1}\right)\left(1 + \frac{R_L}{r_{ds1}}\right) \cong \frac{1}{g_{m1}}\left(1 + \frac{R_L}{r_{ds1}}\right)$$

Comparison of the impedances



Chapter 3 Figure 11





Chapter 3 Figure 08

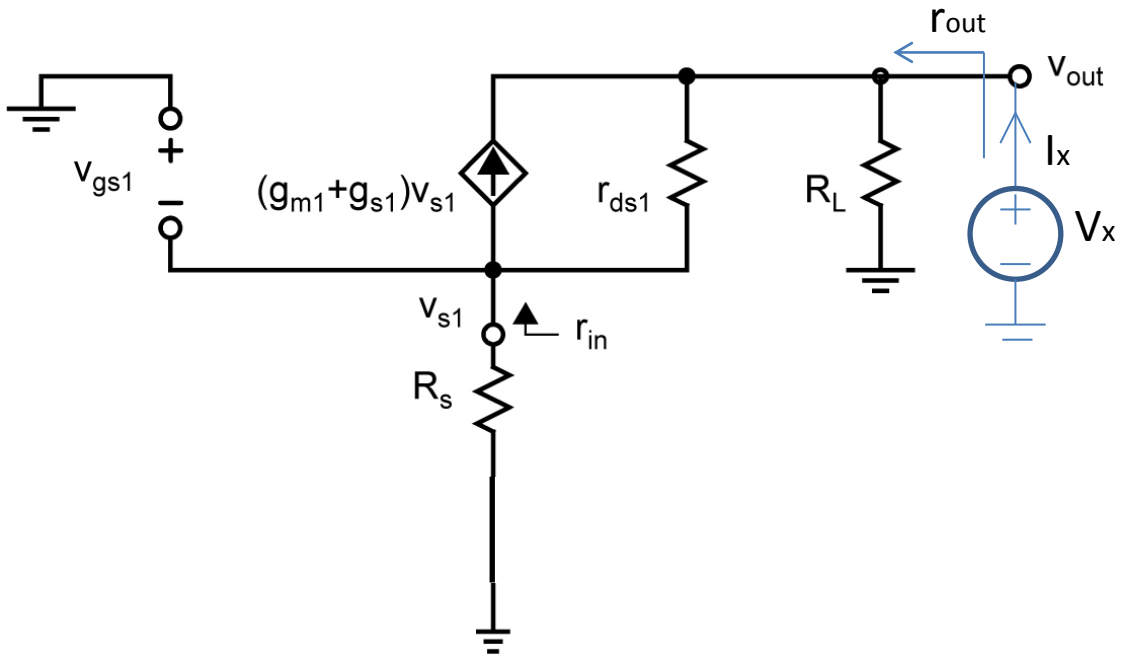
$$g_{in} \equiv \frac{i_s}{v_{s1}} \equiv \frac{g_{m1}+g_{s1}+g_{ds1}}{1+\dfrac{g_{ds1}}{G_L}}$$

$$r_{in} = \frac{1}{g_{in}} = \left(\frac{1}{g_{m1}} \,\|\, \frac{1}{g_{s1}} \,\|\, r_{ds1}\right)\left(1+\frac{R_L}{r_{ds1}}\right) \cong \frac{1}{g_{m1}}\left(1+\frac{R_L}{r_{ds1}}\right)$$

Compare to Slide 16

If $R_L=r_{ds2}=r_{ds1}$, $r_{in}=2/g_{m1}$ for low frequency. If R_L is even larger, then r_{in} is more than $2/g_{m1}$.

Small-signal analysis of CG: r_{out}



Chapter 3 Figure 11

$I_x = V_x/R_L - (g_{m1}+g_{s1})V_{s1} + (V_x-V_{s1})/r_{ds1}$

$-(g_{m1}+g_{s1})V_{s1} + (V_x-V_{s1})/r_{ds1} = V_{s1}/R_s$

$$r_{out} = \frac{V_X}{I_X} = \frac{[1+(g_m+g_{s1})R_S + \frac{R_S}{r_{ds1}}]r_{ds1}R_L}{R_L + r_{ds1}}$$

If $R_L=r_{ds2}=r_{ds1}$ and $R_s=0$, then not surprisingly $r_{out}=r_{ds1}/2$

Example 3.5 (page 127)

Design the common-gate amplifier of Fig. 3.9 to have an input impedance of approximately 50 Ω using the 0.18-μm CMOS devices in Table 1.5 with $I_{bias} = 100\ \mu A$, $(W/L)_3 = 2\ \mu m/0.2\ \mu m$.

Since $(\lambda L)_1 = (\lambda L)_2$, if we take $L_1 = L_2 = 0.2\ \mu m$ we ensure $r_{ds2} = R_L = r_{ds1}$

$r_{in} \cong 2/g_{m1}$

Hence, to ensure $r_{in} = 50\ \Omega$,

$$g_{m1} \cong 2/(50\ \Omega) = 40\ mA/V$$

If we take $V_{eff1} = 200\ mV$,

$$I_{D2} = I_{D1} = g_{m1}V_{eff1}/2 = (40\ mA/V)(200\ mV)/2 = 4\ mA$$

This requires the current mirror to provide a gain of $4\ mA/100\ \mu A = 40$.

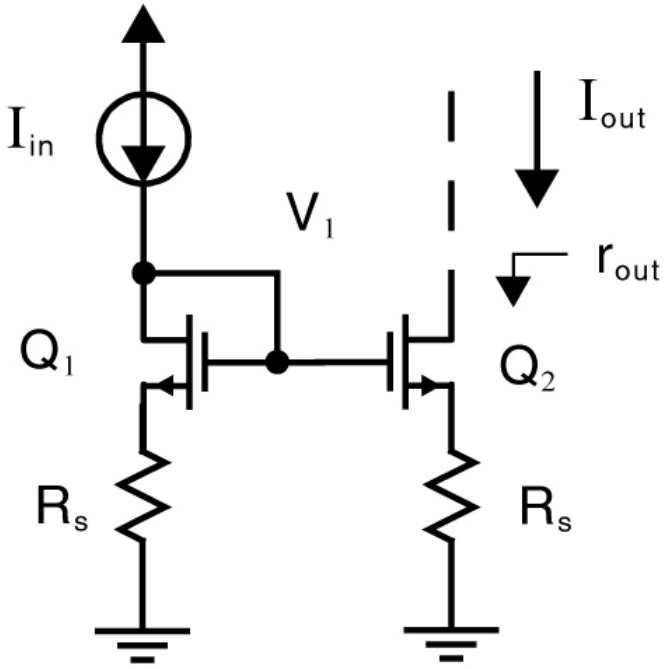
$$(W/L)_2 = 40(W/L)_3 = 80\ \mu m/0.2\ \mu m$$

$$(W/L)_1 = \frac{g_{m1}^2}{2\mu_n C_{ox} I_{D1}} = 148\ \mu m/0.2\ \mu m$$

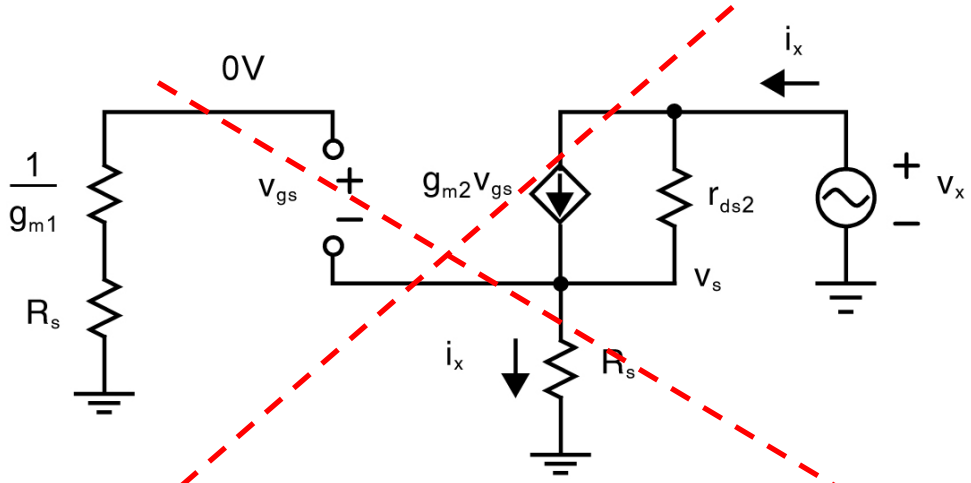
0.18 μm	
NMOS	**PMOS**
270	70
0.45	–0.45
0.08	0.08
8.5	8.5
5	5
1.6	1.7
1.7	1.0
1.6	2.4
0.35	0.35
0.50	0.55

3.5 Source-degenerated current mirrors

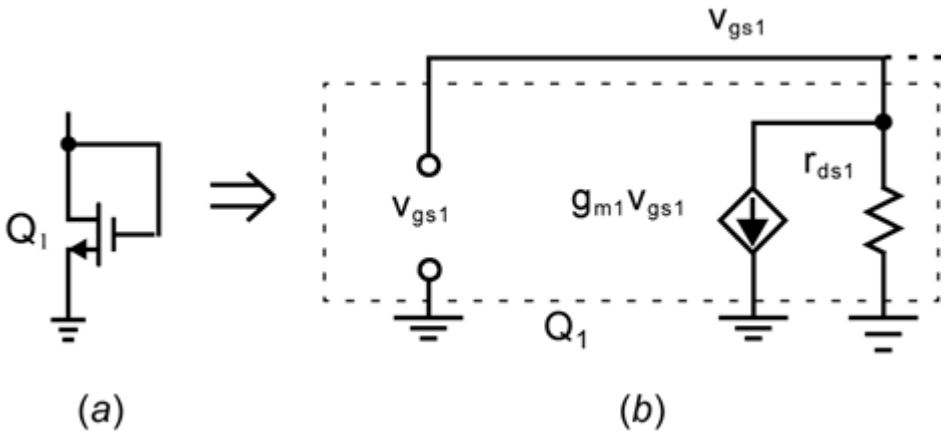
Simple current mirrors presented before have relatively small output impedance.
To increase this output impedance, a source degenerated current mirror can be used.



Chapter 3 Figure 12



Chapter 3 Figure 13



Small-signal model to find r_{out}

Note that in the small-signal model to compute r_{out}, (1) the gate voltage for both Q1 and Q2 is 0 as no small-signal current flows to the gate, (2) we neglect the body effect.

$$v_s = i_x R_s$$

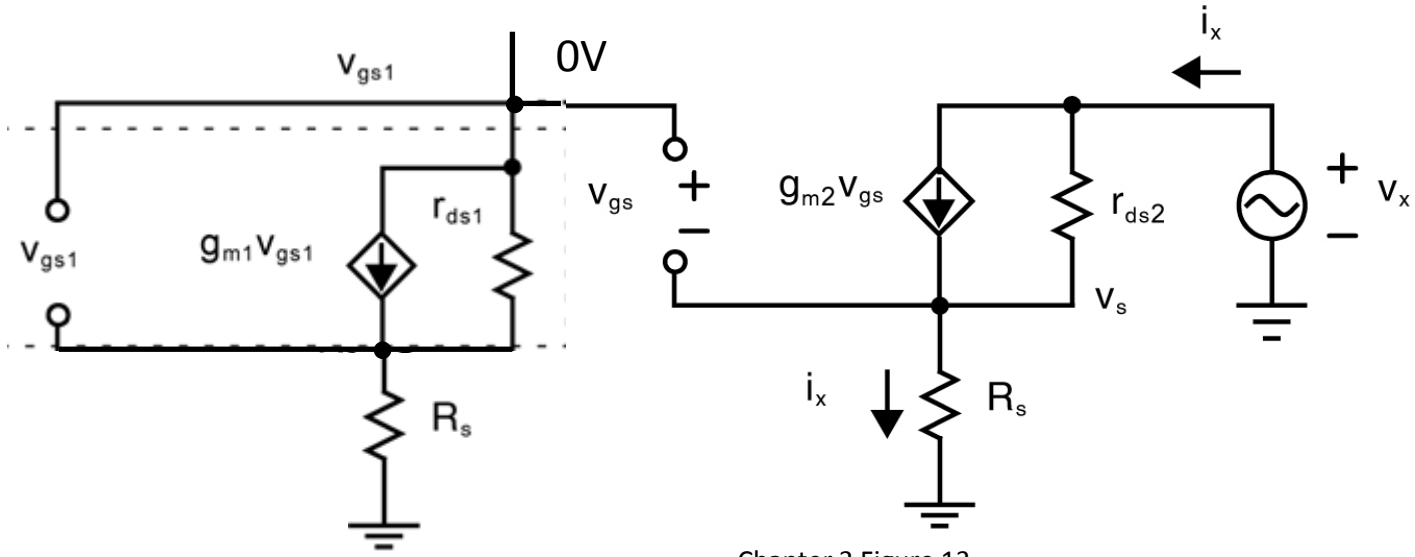
$$v_{gs} = -v_s \quad \leftarrow \quad g_{m1}V_{gs1} = V_{gs1}/r_{ds1}$$

$$i_x = g_{m2}v_{gs} + \frac{v_x - v_s}{r_{ds2}} \qquad i_x = -i_x g_{m2} R_s + \frac{v_x - i_x R_s}{r_{ds2}}$$

Compare to Slides 22

$$r_{out} = \frac{v_x}{i_x} = r_{ds2}[1 + R_s(g_{m2} + g_{ds2})] \cong r_{ds2}(1 + R_s g_{m2}) \cong r_{ds2}[1 + R_s(g_{m2} + g_{s2})]$$

If body effect included



Chapter 3 Figure 13

Example 3.6 (page 128)

Consider the current mirror shown in Fig. 3.12, where $I_{in} = 100\ \mu A$, each transistor has $W/L = 10\ \mu m/0.2\ \mu m$, and $R_s = 1\ k\Omega$. Using the 0.18-μm CMOS devices in Table 1.5, find r_{out} for the current mirror. Assume the body effect can be approximated by $g_s = 0.15 g_m$.

Nominally, $I_{out} = I_{in}$, and thus we find the small-signal parameters for this current mirror to be

$$g_{m2} = \sqrt{2\mu_n C_{ox}(W/L)I_{out}} = 1.64\ mA/V$$

Also we have

$$r_{ds2} = \frac{0.2\ \mu m}{0.08\ \mu m/V\ 100\ \mu A} = 25\ k\Omega$$

$$r_{out} = 25\ k\Omega\left[1 + 1\ k\Omega\left(1.64\ mA/V + 0.15 \cdot 1.64\ mA/V + \frac{1}{25\ k\Omega}\right)\right] = 73.15\ k\Omega$$

Also note that the voltage drop across R_s equals $100\ \mu A \times 1\ k\Omega = 0.1\ V$

Therefore, compared to the simple two-transistor current mirror, the output impedance of source-degenerated current mirror has output impedance increased by a factor equal to $(1+g_{m2}R_s)$.

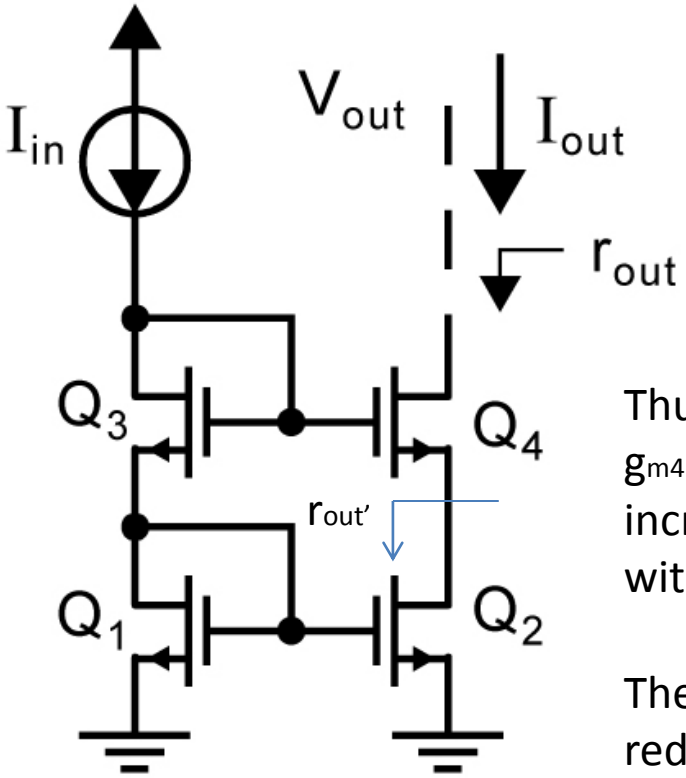
Note also that such a formula can often be applied to moderately complicated circuits to quickly estimate the impedance looking into a node.

3.6 Cascode current mirrors

Cascode current mirrors can be used to further increase the output impedance.

Note that r_{out}' looking into the drain of Q2 is simply r_{ds2}.

The r_{out} looking into the drain of Q4, can be derived from the formula for source-degenerated current mirrors, by considering Q4 as a current source with a source-degenerated resistor of rds2 from Q2.



Chapter 3 Figure 14

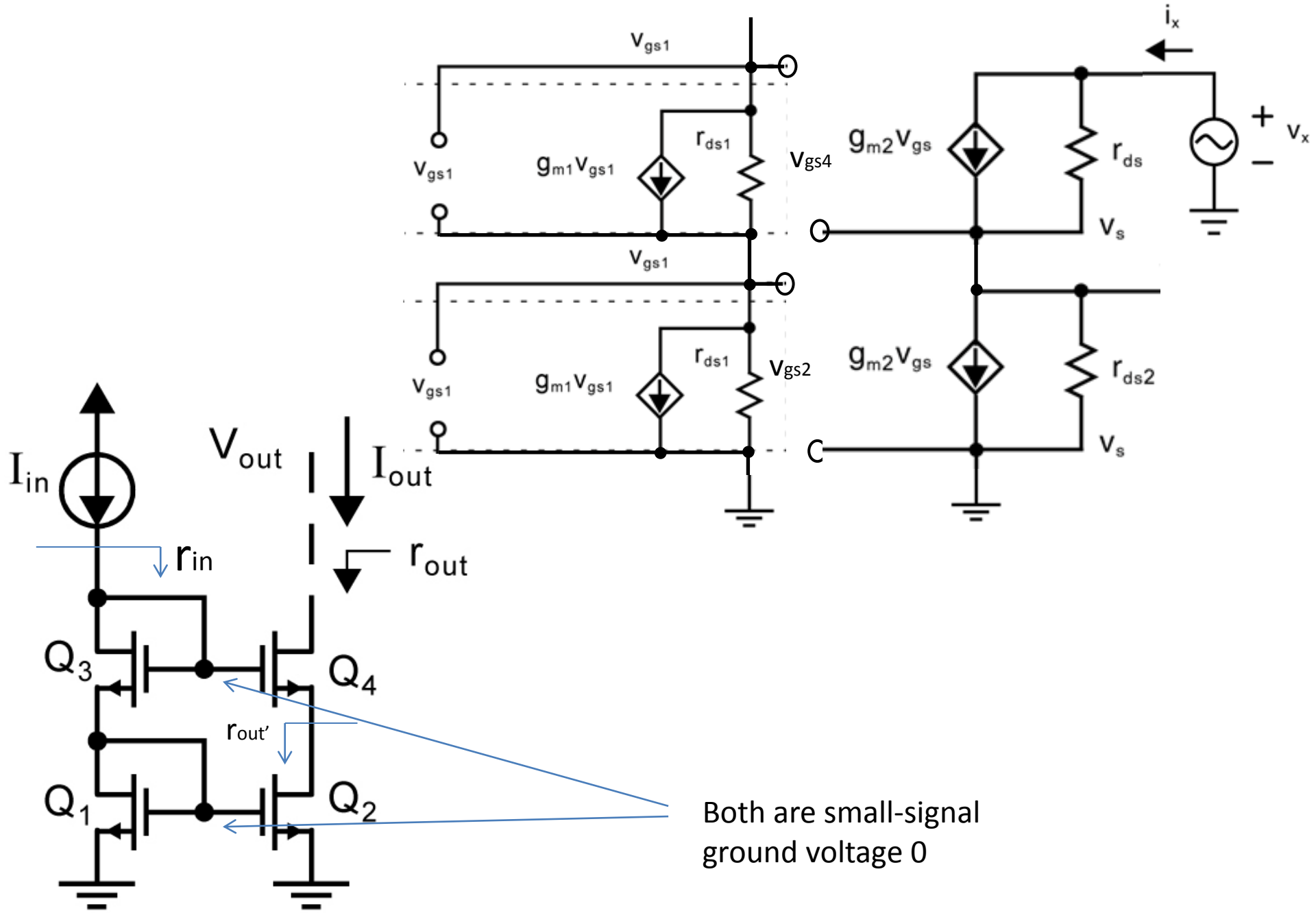
$$r_{out} = r_{ds4}[1 + R_s(g_{m4} + g_{s4} + g_{ds4})]$$

where now $R_s = r_{ds2}$. Therefore, the output impedance is given by

$$r_{out} = r_{ds4}[1 + r_{ds2}(g_{m4} + g_{s4} + g_{ds4})]$$
$$\cong r_{ds4}[1 + r_{ds2}(g_{m4} + g_{s4})]$$
$$\cong r_{ds4}(r_{ds2}g_{m4})$$

Thus, the output impedance is increased by a factor of $g_{m4}r_{ds4}$, which is the gain of a single transistor. Such a large increase can be important to realize single-stage amplifiers with large gains.

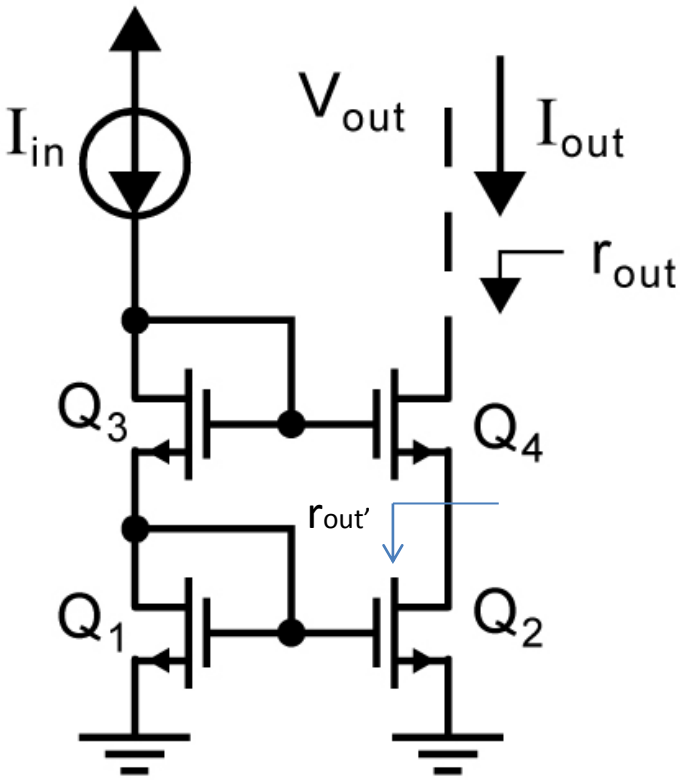
The drawback in using a cascode current mirror is the reduction of the maximum output voltage swing.



Chapter 3 Figure 14

Minimum output voltage

What is the minimum voltage at V_{out} to maintain Q2 and Q4 in active region? If we assume all transistors have the same sizes and currents, and therefore the same $V_{gsi}=V_{effi}+V_{tni}$, where i=1,2,3,4, then



Chapter 3 Figure 14

$$V_{G3} = V_{GS1} + V_{GS3} = 2V_{eff} + 2V_{tn}$$

$$V_{DS2} = V_{G3} - V_{GS4} = V_{G3} - (V_{eff} + V_{tn}) = V_{eff} + V_{tn}$$

So, the V_{ds2} for Q2 is larger than the minimum needed which is V_{eff2}.

Since the smallest output voltage V_{D4} can be $V_{DS2}+V_{eff2}$ before Q4 goes into triode region, so the minimum allowed voltage for V_{out} is

$$V_{out} > V_{DS2} + V_{eff} = 2V_{eff1} + V_{tn}$$

The loss of signal swing is a serious drawback when modern analog IC are used with low power supply of 1V. (Later, we will see how to address this issue).

Example 3.7 (page 130)

Consider the cascode current mirror shown in Fig. 3.14, where $I_{in} = 100\ \mu A$ and each transistor has $W/L = 10\ \mu m/0.4\ \mu m$. Given the 0.35-μm CMOS device parameters in Table 1.5, find r_{out} for the current mirror (approximating the body effect by $0.2g_m$). Also find the minimum output voltage at V_{out} such that the output transistors remain in the active region.

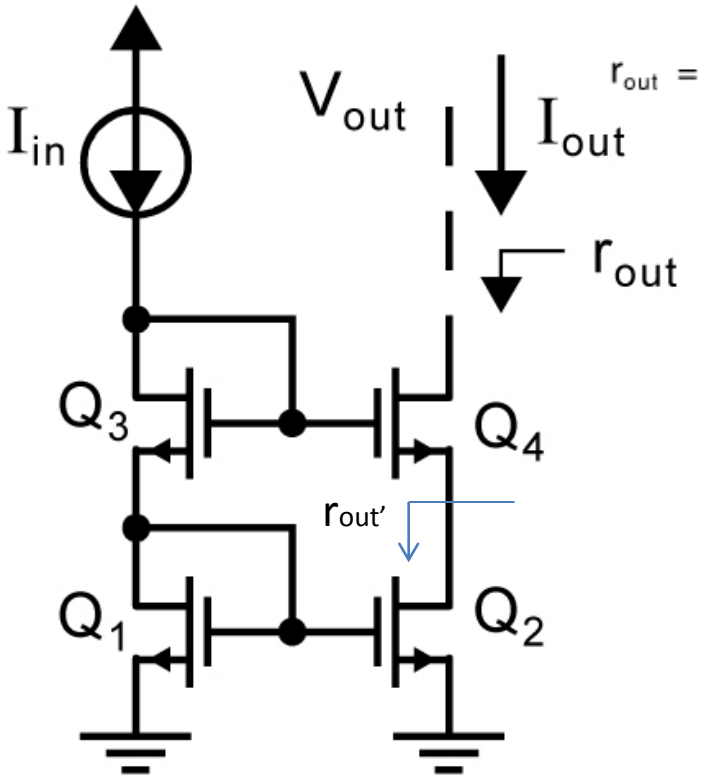
Nominally, $I_{out} = I_{in}$, and thus we can find the small-signal parameters for this current mirror to be

$$g_{m4} = \sqrt{2\mu_n C_{ox}(W/L)I_{out}} = 0.97\ mA/V$$

$$r_{ds2} = r_{ds4} = \frac{0.4\ \mu m}{0.16\ \mu m/V\ 100\ \mu A} = 25\ k\Omega$$

$$r_{out} = 25\ k\Omega[25\ k\Omega(0.97\ mA/V + 0.2 \times 0.97\ mA/V + 1/25\ k\Omega)] = 753\ k\Omega$$

$$V_{eff} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)}} = 0.205\ V$$



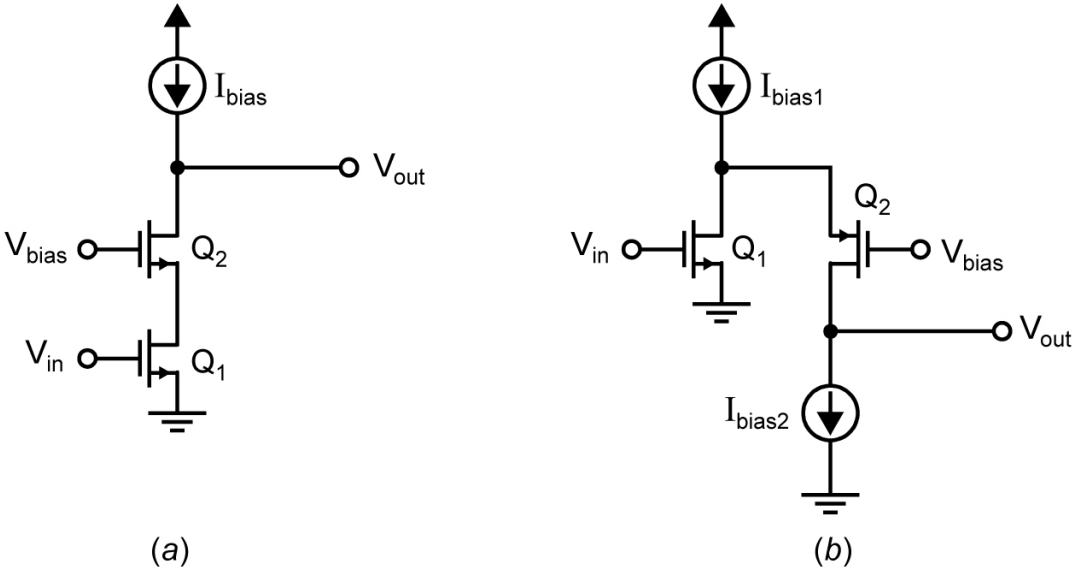
Chapter 3 Figure 14

So the minimum V_{out} is then $2V_{eff} + V_{tn} = 0.98V$, which 0.77V larger than the simple current mirror while rout is increased by 30 times.

3.7 Cascode gain stage

In modern IC design, a commonly used configuration for a single-stage amplifier is a cascode amplifier. This configuration consists of a CS transistor feeding into a CG one.
In (a) below, both CS Q1 and cascode transistor Q2 are NMOS (telescopic-cascode amplifier)
In (b), CS Q1 is NMOS and cascode transistor Q2 is PMOS (folded-cascode amplifier).

Two major reasons for cascode stages: (1) they provide large gain when current sources are realized with cascode current mirrors; (2) they limit the voltage across Q1, minimizing short channel effects.
The main drawback of cascode stages is that the output voltage swing is reduced in order to keep both Q1 and Q2 in active region when compared to the CS amplifier.



Chapter 3 Figure 15

Small-signal model

The gain from the input to the source of Q_2 is simply that of a common-source amplifier with a load resistance of r_{in2} and is therefore given by

$$\frac{v_{s2}}{v_{in}} = -g_{m1}(r_{ds1} \| r_{in2}) = -\frac{g_{m1}}{g_{ds1} + g_{in2}} \qquad (3.52)$$

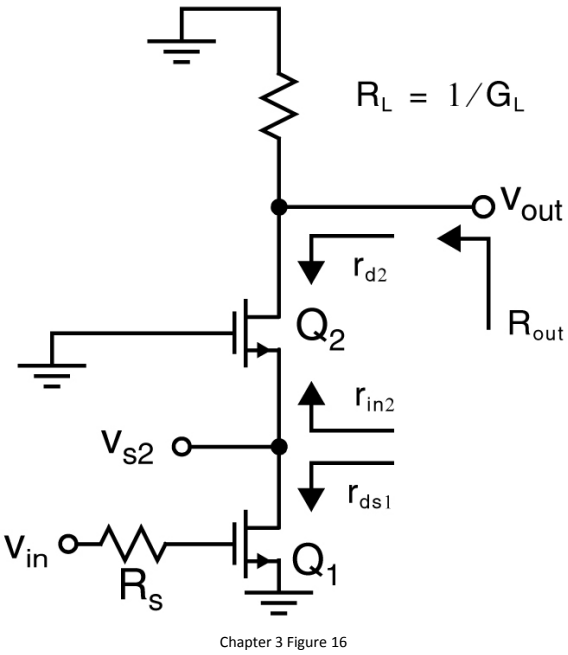
The impedance looking into source of Q2

$$g_{in2} = 1/r_{in2} = \frac{g_{m2} + g_{s2} + g_{ds2}}{1 + \dfrac{R_L}{r_{ds2}}} \cong \frac{g_{m2}}{1 + \dfrac{R_L}{r_{ds2}}}$$

The gain from the source of Q_2 to the output is simply that derived earlier for the common-gate stage.

$$\frac{v_{out}}{v_{s2}} = \frac{g_{m2} + g_{s2} + g_{ds2}}{g_{ds2} + G_L}$$

$$\cong g_{m2}(r_{ds2} \| R_L) = \frac{g_{m2}}{(g_{ds2} + G_L)}$$



Chapter 3 Figure 16

The overall gain is

$$A_V = \frac{v_{s2}}{v_{in}}\frac{v_{out}}{v_{s2}} \cong -g_{m1}g_{m2}(r_{ds1} \| r_{in2})(r_{ds2} \| R_L)$$

The impedance looking into drain of Q2

$$r_{d2} \cong g_{m2}r_{ds1}r_{ds2}$$

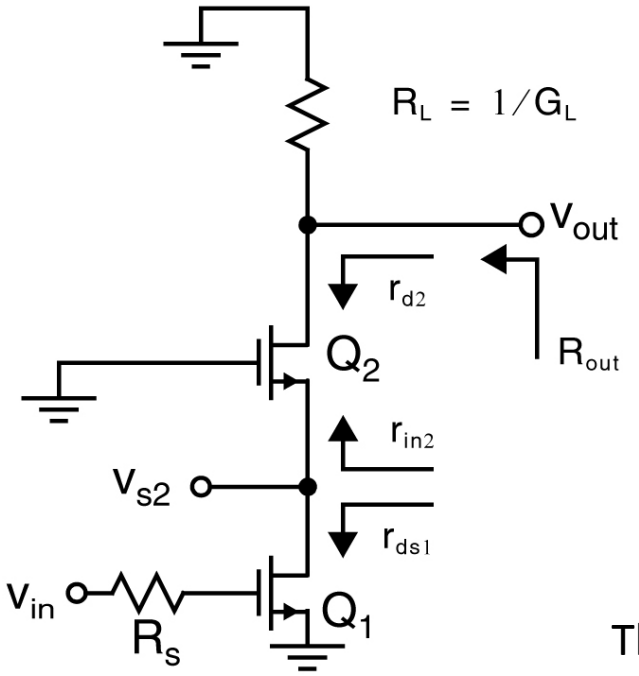
The total output resistance will be

$$R_{out} = r_{d2} \| R_L$$

Example 3.9 (page 133)

Find approximate expressions for the gain and output resistance of the cascode stage in Fig. 3.15(*a*) assuming I_{bias} is a simple current source with an output impedance on the order of $R_L \approx r_{ds\text{-}p}$
Compute approximate numerical results assuming all transistors have g_m on the order of 0.5mA/V and r_{ds} on the order of 100kΩ.

We shall drop the indices for all small-signal values under the assumption that the transistors are somewhat matched and to simplify matters since we are only deriving an approximate answer.



Chapter 3 Figure 16

$$g_{in2} \approx \frac{1}{2} g_m \Rightarrow r_{in2} \approx \frac{2}{g_m}$$

Assuming r_{ds1} is much larger than r_{in2}, the gain

$$\frac{v_{s2}}{v_{in}} \approx -\frac{g_m}{g_m/2} = -2$$

$$\frac{v_{out}}{v_{s2}} \approx \frac{1}{2} g_m r_{ds}$$

$$A_V = \frac{v_{s2}}{v_{in}} \cdot \frac{v_{out}}{v_{s2}} \approx -g_m r_{ds}$$

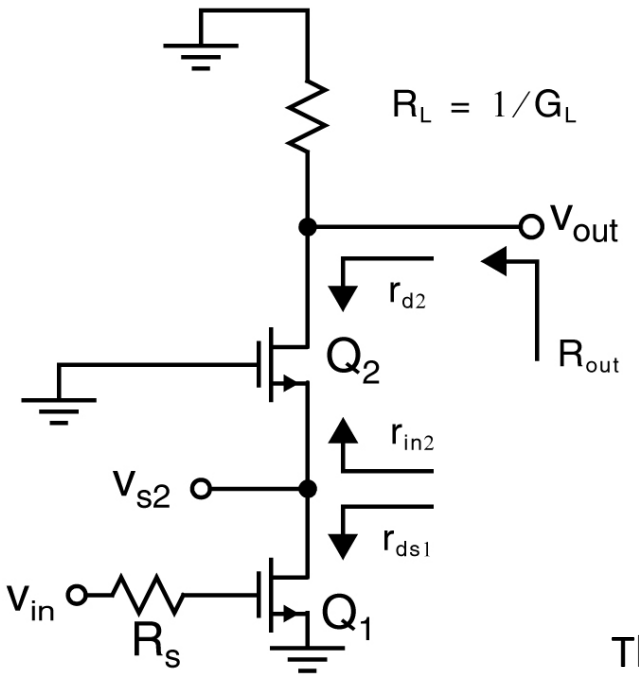
Since $R_L \ll r_{d2}$, the output resistance is $R_{out} \approx r_{ds}$

The gain in this case is only a factor of 2 larger than that for a common-source amplifier.
Also, almost all of the gain is across Q2.

Example 3.10 revised (page 135)

Find approximate expressions for the gain and output resistance of the cascode stage in Fig. 3.15(*a*) assuming I_{bias} is a simple current source with an output impedance on the order of $R_L \approx g_{m\text{-}p} r_{ds\text{-}p}^2 \approx g_m r_{ds}^2$
Compute approximate numerical results assuming all transistors have g_m on the order of 0.5mA/V and r_{ds} on the order of 100kΩ.

We shall drop the indices for all small-signal values under the assumption that the transistors are somewhat matched and to simplify matters since we are only deriving an approximate answer.



Chapter 3 Figure 16

$$g_{in2} = 1/r_{in2} \approx \frac{g_m}{1 + g_{ds} g_m r_{ds}^2} \cong g_{ds}$$

$$\Rightarrow r_{in2} \approx r_{ds}$$

$$\frac{v_{s2}}{v_{in}} \approx -\frac{1}{2} g_m r_{ds}$$

since $R_L \gg r_{ds2}$, $\quad \frac{v_{out}}{v_{s2}} \approx g_m r_{ds}$

$$A_V \approx -\frac{1}{2} g_m^2 r_{ds}^2 = -\frac{1}{2}\left(\frac{g_m}{g_{ds}}\right)^2$$

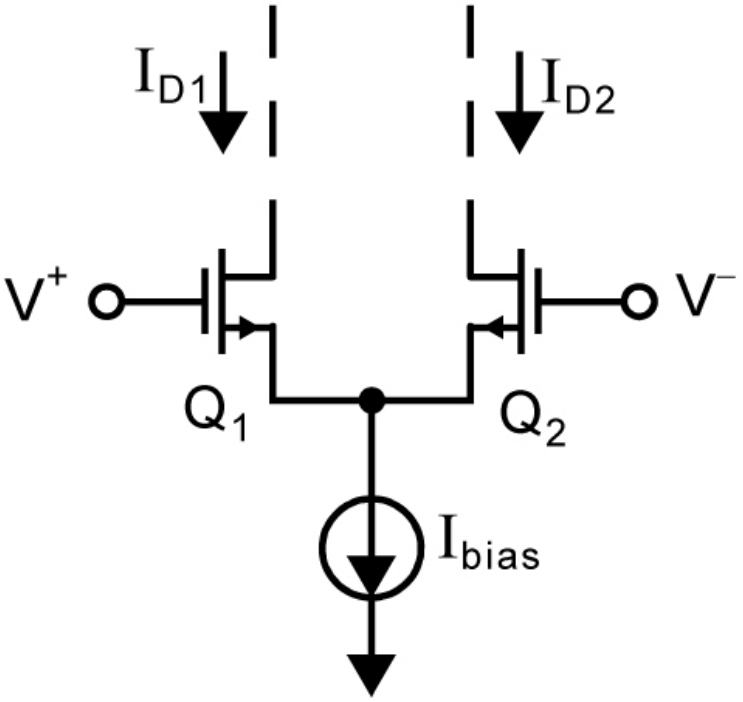
$$R_{out} = R_L \| r_{d2} \approx \frac{1}{2} g_m r_{ds}^2$$

The gain and output resistance is dramatically improved compared to the previous example when a cascode current mirror is used for I_{bias}.

3.8 Differential pair and gain stage

A differential pair have identically-sized and –biased transistors Q1 and Q2.

It is usually used as the input stage of a Operational Amplifier.



Small-signal model using T model

To simplify the analysis, we ignore the output impedance of the transistors temporarily. Defining the differential input voltage as $v_{in} \equiv v^+ - v^-$.

$$i_{d1} = i_{s1} = \frac{v_{in}}{r_{s1} + r_{s2}} = \frac{v_{in}}{1/g_{m1} + 1/g_{m2}}$$

Since both Q_1 and Q_2 have the same bias currents, $g_{m1} = g_{m2}$.

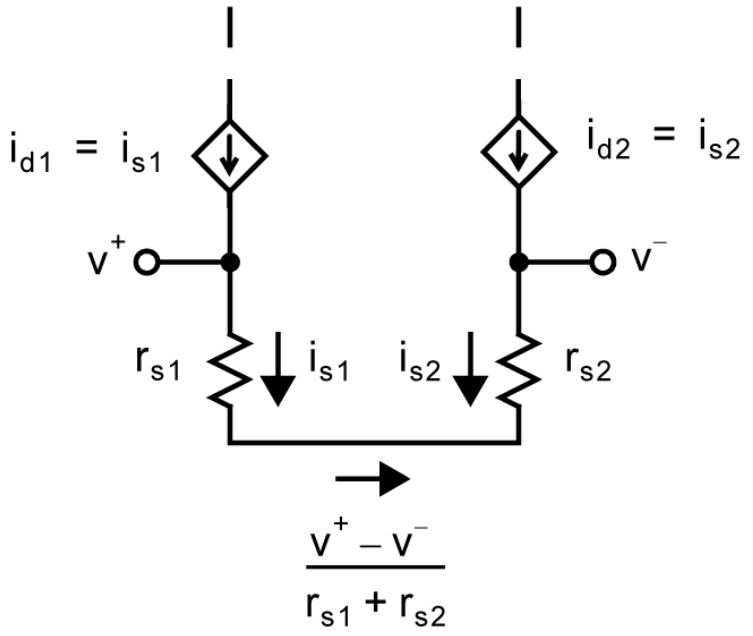
$$i_{d1} = \frac{g_{m1}}{2} v_{in}$$

Also, since $i_{d2} = i_{s2} = -i_{d1}$,

$$i_{d2} = -\frac{g_{m1}}{2} v_{in}$$

Finally, defining a differential output current, $i_{out} \equiv i_{d1} - i_{d2}$, the following relationship is obtained:

$$i_{out} = g_{m1} v_{in}$$

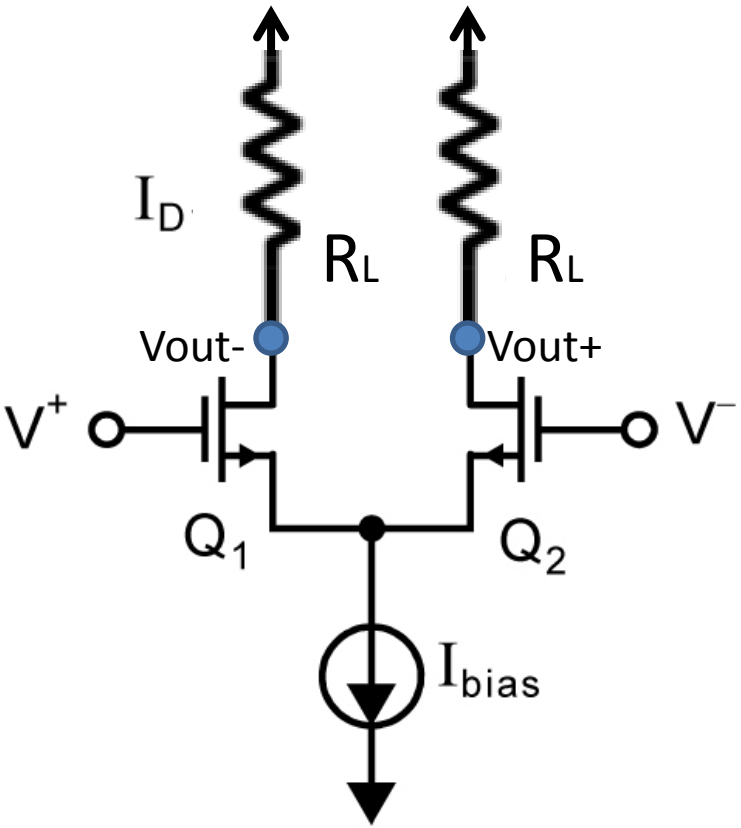


Chapter 3 Figure 18

Differential pair with resistive load

If two resistive loads R_L are connected between the drains of Q_1 and Q_2 and a positive supply, the result is a differential output voltage between the two drain nodes, $v_{out} = (g_{m1}R_L)v_{in}$ and the stage has a differential small-signal gain of $g_{m1}R_L$.

Note that r_{ds} is neglected.

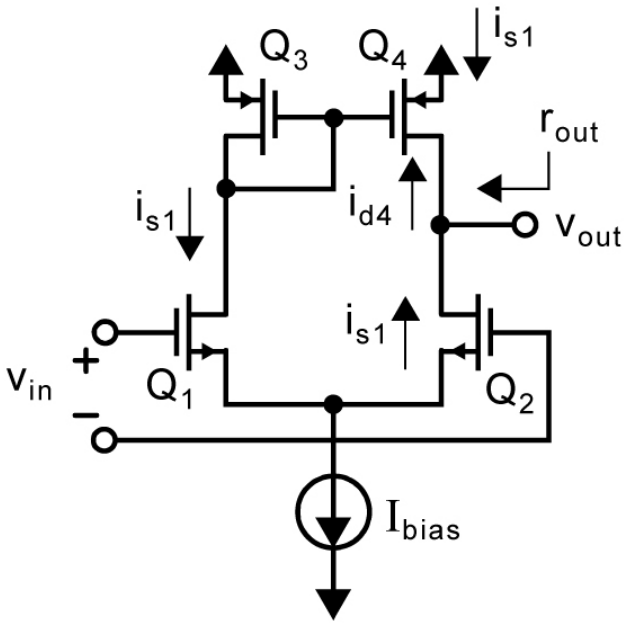


Chapter 3 Figure 17

Differential pair with current mirror

As with the CS amplifier, we can replace the resistor by current mirrors as an active load. Then, a complete differential-input, single-ended output gain stage can be realized. This circuit is typically the first gain stage in a classical two-stage integrated OpAmp to be discussed later.

From small-signal analysis of the differential pair,



Chapter 3 Figure 19

$$i_{d1} = i_{s1} = \frac{g_{m1}}{2} v_{in}$$

$$i_{d4} = i_{d3} = -i_{s1}$$

$$i_{d2} = -i_{s1},$$

$$v_{out} = (-i_{d2} - i_{d4}) r_{out} = 2 i_{s1} r_{out} = g_{m1} r_{out} v_{in}$$

How to determine the small-signal output resistance r_{out}?

Computing r_{out}

T model was used for Q1, Q2 and diode-connected Q3 was replaced by an equivalent resistance and hybrid-pi model for Q4.

$$i_x = i_{x1} + i_{x2} + i_{x3} + i_{x4}.$$

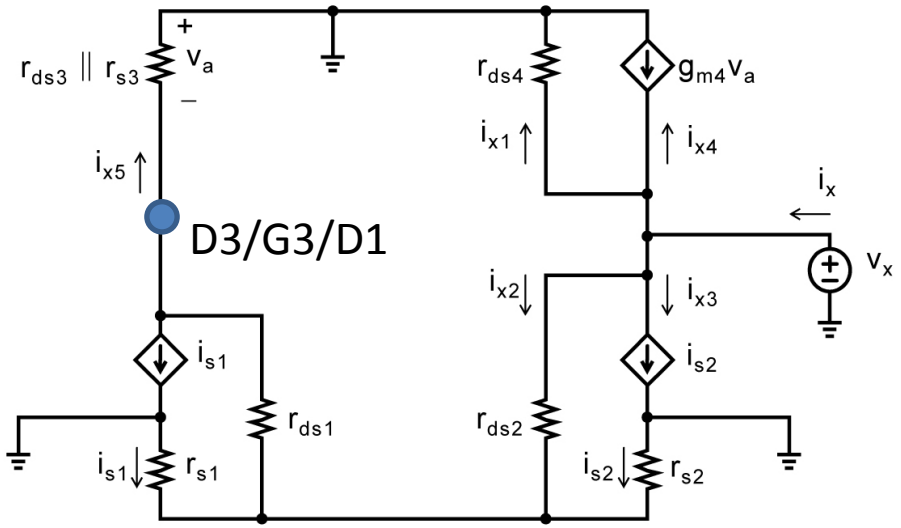
$$i_{x1} = \frac{v_x}{r_{ds4}}$$

Then assuming the effect of r_{ds1} can be ignored (since it is much larger than r_{s1}), then

$$i_{x2} \cong \frac{v_x}{r_{ds2} + (r_{s1} \parallel r_{s2})} \cong \frac{v_x}{r_{ds2}} \quad \text{since } r_{ds2} \text{ is typically much greater than } r_{s1} \parallel r_{s2}.$$

This i_{x2} current splits equally between i_{s1} and i_{s2} (assuming $r_{s1} = r_{s2}$ and once again ignoring r_{ds1}),

$$i_{s1} = i_{s2} = \frac{-v_x}{2r_{ds2}}$$



Chapter 3 Figure 20

Computing r_{out}

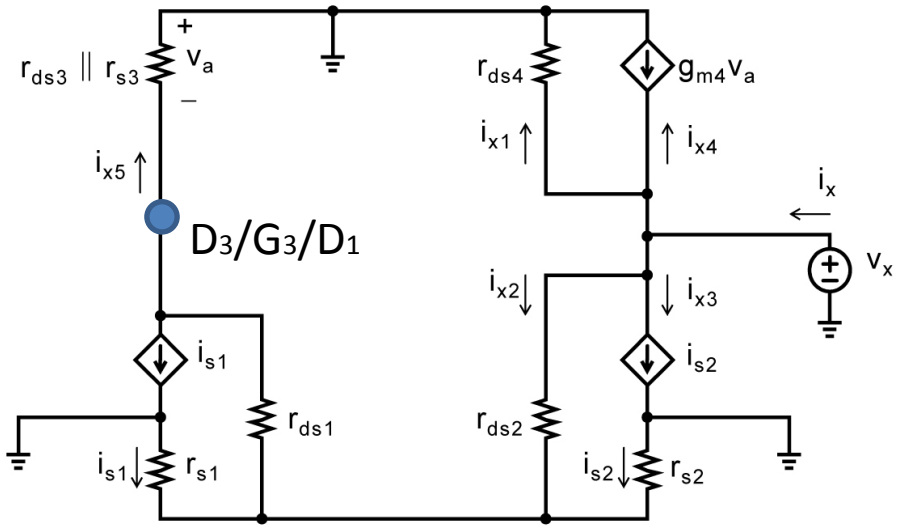
However, since the current mirror realized by Q_3 and Q_4 results in $i_{x4} = i_{x5}$ (assuming $g_{m4} = 1/r_{s4} = 1/r_{s3}$ and r_{ds3} is much larger than r_{s3}), the current i_{x4} is given by

$$i_{x4} = -i_{s1} = -i_{s2} = -i_{x3}$$

$$r_{out} = \frac{v_x}{i_{x1} + i_{x2} + i_{x3} + i_{x4}} = \frac{v_x}{(v_x/r_{ds4}) + (v_x/r_{ds2})}$$

$$r_{out} = r_{ds2} \parallel r_{ds4}$$

$$A_v = g_{m1}(r_{ds2} \parallel r_{ds4})$$



Chapter 3 Figure 20