6.3 Advanced current mirrors: wide-swing

Q3 and Q4 acts like a single-diode connected transistor to create the gate source voltage for Q3. Including Q4 helps lower the V_{ds3} so that it matches V_{ds2}. Other than that, Q4 has little effect on the circuit's operation.

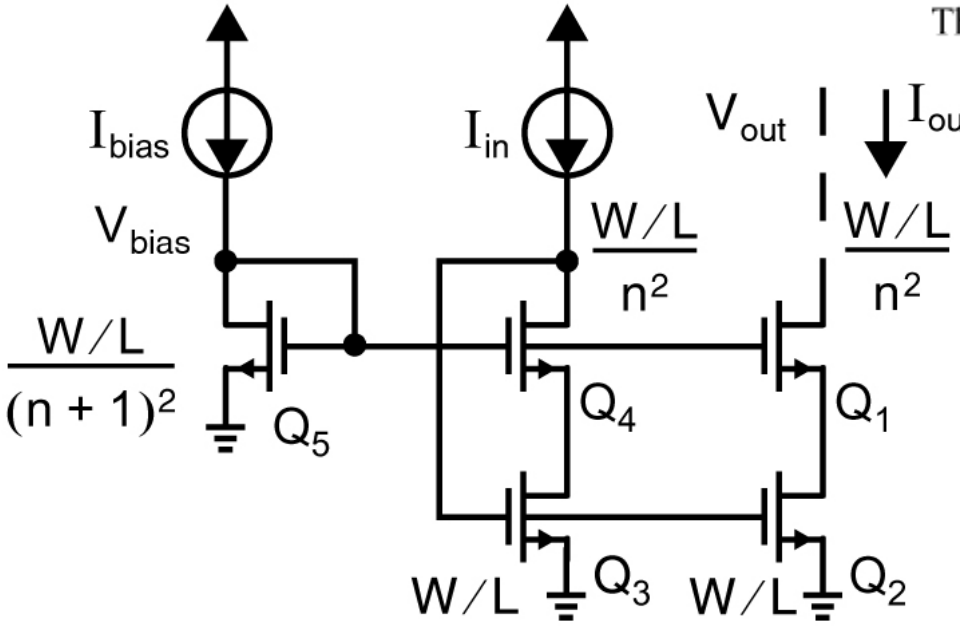
$$V_{eff} = V_{eff2} = V_{eff3} = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}(W/L)}}$$ Assume $I_{D2}=I_{D3}=I_{D5}$

since Q_5 has the same drain current but is $(n+1)^2$ times smaller, $V_{eff5} = (n+1)V_{eff}$ $V_{eff1} = V_{eff4} = nV_{eff}$

Thus, $V_{G5} = V_{G4} = V_{G1} = (n+1)V_{eff} + V_{tn}$

Furthermore, $V_{GS1}=V_{GS4} \longrightarrow V_{DS2} = V_{DS3} = V_{G5} - V_{GS1} = V_{G5} - (nV_{eff} + V_{tn}) = V_{eff}$

This drain-source voltage puts both Q_2 and Q_3 right at the edge of the triode region.



Thus, the minimum allowable output voltage is now

$V_{out} > V_{eff1} + V_{eff2} = (n+1)V_{eff}$

$V_{out} > 2V_{eff}$ If n=1

Also we need $V_{DS4} > V_{eff4} = nV_{eff}$

$V_{DS4} = V_{G3} - V_{DS3} = (V_{eff} + V_{tn}) - V_{eff} = V_{tn}$

not a difficult requirement.

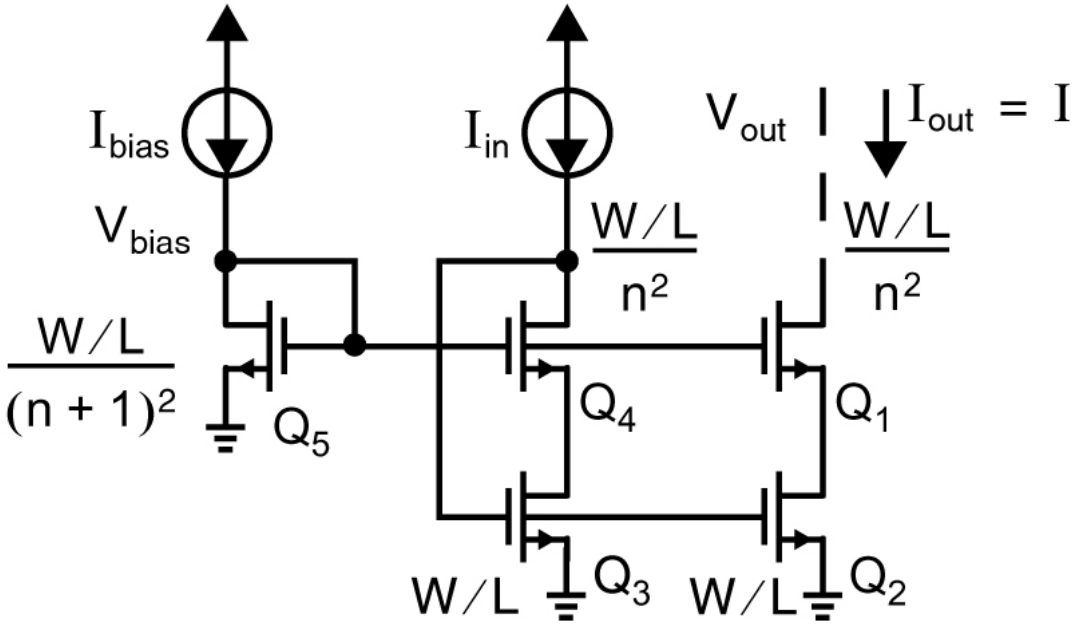
Chapter 6 Figure 12

6.3 Advanced current mirrors: wide-swing

In most applications, it is desirable to make (W/L)5 smaller than that given in the Figure so that Q2 and Q3 can be biased with a slightly larger V_{ds}. This would help counter the body effect of Q1 an Q4, which have their V_t increased.

To save power consumption, I_{bias} and Q5 size can be scaled down a little bit while keeping the same gate voltage.

Also, it may be wise to make the length of Q3 and Q2 larger than the minimum and that of Q1 and Q4 even larger since Q1 often sees a larger voltage V_{out}. This helps reduce short-channel effects.



Chapter 6 Figure 12

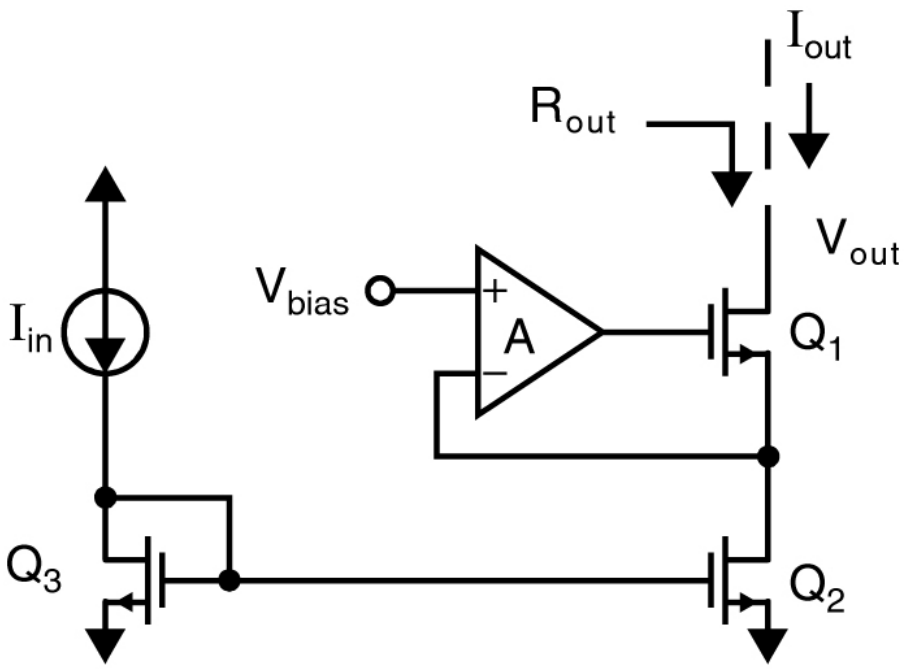
6.3.2 Enhanced output impedance CM and Gain boosting

The basic idea is to use a feedback amplifier to keep the drain-source voltage across Q2 as stable as possible, irrespective of the output voltage.

From small-signal analysis, $I_x=g_m v_{gs}+(V_x-V_s)/r_{ds1}$, $V_{gs}+V_s=A(0-V_s)$, $V_x=I_x*r_{ds2}$

$$R_{out} \cong g_{m1} r_{ds1} r_{ds2} (1 + A)$$

Note that the stability of the feedback loop comprised of A and Q1 must be verified.



Chapter 6 Figure 13

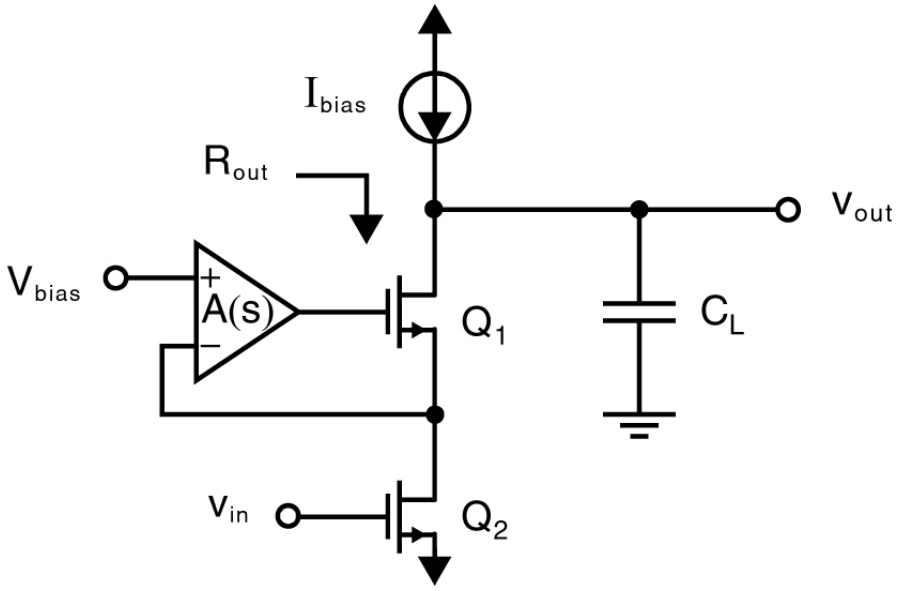
6.3.2 Enhanced output impedance CM and Gain boosting

This technique can also be applied to increase the R_{out} of a cascode gain stage (the small signal current $-g_{m2}v_{in}$ must go through R_{out} and C_L).

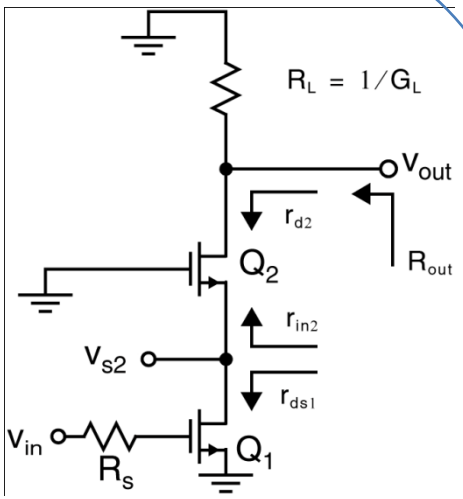
$$A_V(s) = \frac{V_{out}(s)}{V_{in}(s)} = -g_{m2}\left(R_{out}(s) \parallel \frac{1}{sC_L}\right) \qquad R_{out}(s) = g_{m1}r_{ds1}r_{ds2}(1 + A(s))$$

Comparing the DC gain only, it can be seen that it is a factor of (1+A) larger than the conventional cascode amplifier discussed in Chapter 3.

To realize this gain, note that the I_{bias} current source must be similarly enhanced to achieve comparable output impedance as R_{out}.



Chapter 6 Figure 14



Chapter 3 Figure 16

$$R_L \approx g_{m\text{-}p}r_{ds\text{-}p}^2 \approx g_m r_{ds}^2$$

$$A_V \approx -\frac{1}{2}g_m^2 r_{ds}^2 = -\frac{1}{2}\left(\frac{g_m}{g_{ds}}\right)^2$$

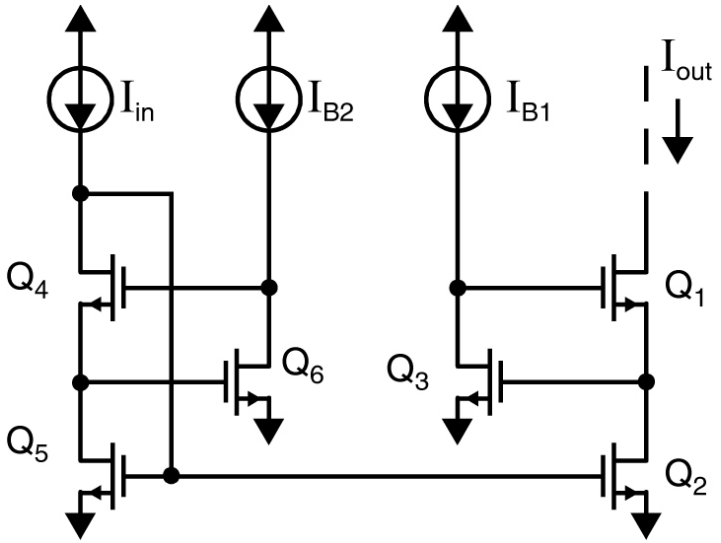
6.3.2 Sackinger's design

The feedback amplifier in this case is realized by transistor Q3 and Q1. Note that Q3 is a CS amplifier, therefore the gain is $g_{m3}r_{ds3}/2$ if I_{B1} has an output impedance of r_{ds3}.

So the total output impedance from the drain of Q1 is: $$r_{out} \cong \frac{g_{m1}g_{m3}r_{ds1}r_{ds2}r_{ds3}}{2}$$

The circuit consisting of Q4, Q5 and Q6, I_{in} and I_{B2} operates likes a diode-connected transistor, but its main purpose is to match those transistors in the output circuitry so that all transistors are biased accurately and $I_{out}=I_{in}$.

One major limitation is that the signal swing is significantly reduced due to Q2 ad Q5 being biased to have drain-source voltages much larger ($V_{DS2} = V_{DS5} = V_{eff3} + V_{tn}$)



Chapter 6 Figure 15

6.3.3. Wide-swing current mirror with enhanced output impedance

Such a circuit is very similar to the Sachinger's design, except that diode-connected transistors used as level shifters Q4 have been added in front of the CS amplifiers.

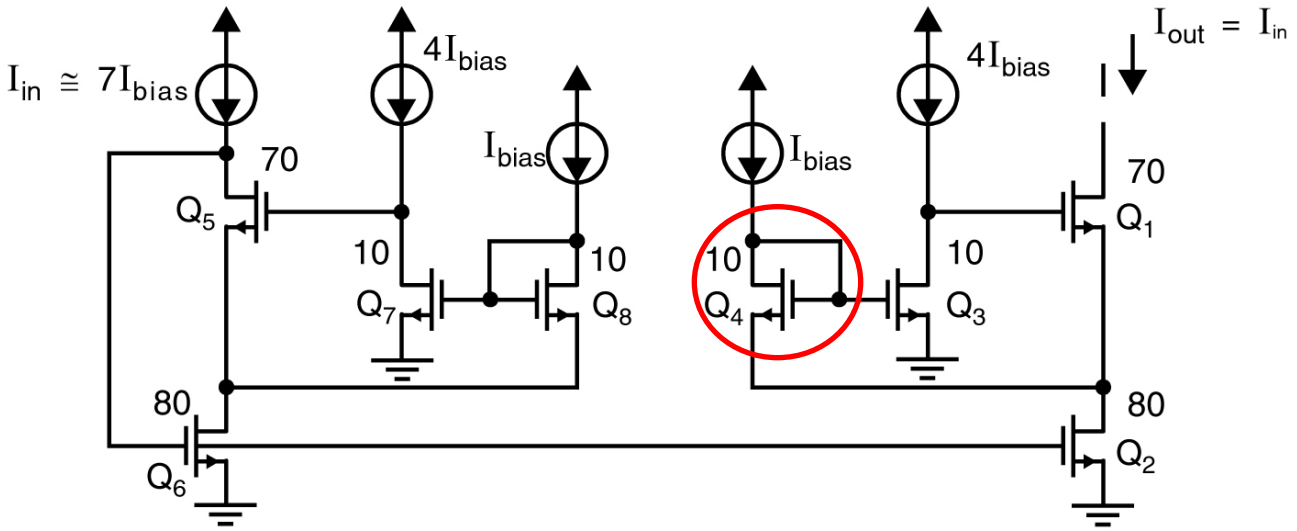
The current density of most transistors (except Q3 and Q7) are about the same, V_{eff}, and that of Q3, Q7, $2V_{eff}$. So

$$V_{G3} = 2V_{eff} + V_{tn}$$

$$V_{DS2} = V_{S4} = V_{G3} - V_{GS4} = (2V_{eff} + V_{tn}) - (V_{eff} + V_{tn}) = V_{eff}$$

$$V_{out} > V_{DS2} + V_{eff1} = 2V_{eff}$$

Two issues with this circuit: 1. power consumption may be large, 2 additional poles introduced by the enhanced circuitry may be at lower frequencies.



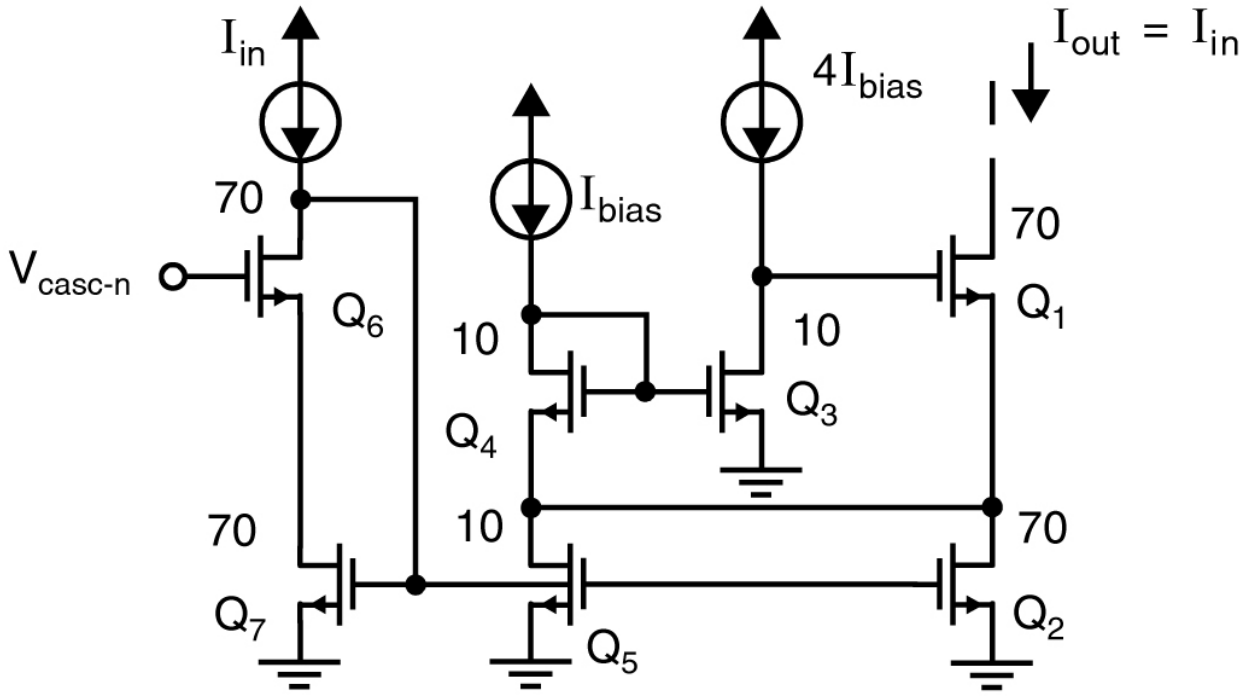
Chapter 6 Figure 16

6.3.3. Wide-swing current mirror with enhanced output impedance

A variation of the previous circuit is shown below. It reduces the power, but matching is poorer.

Note that Q2 in previous circuit is split to Q2 and Q5 in this circuit.

It is predicted that this current mirror may be more used when power supply voltage is smaller or larger gains are desired.



Chapter 6 Figure 17

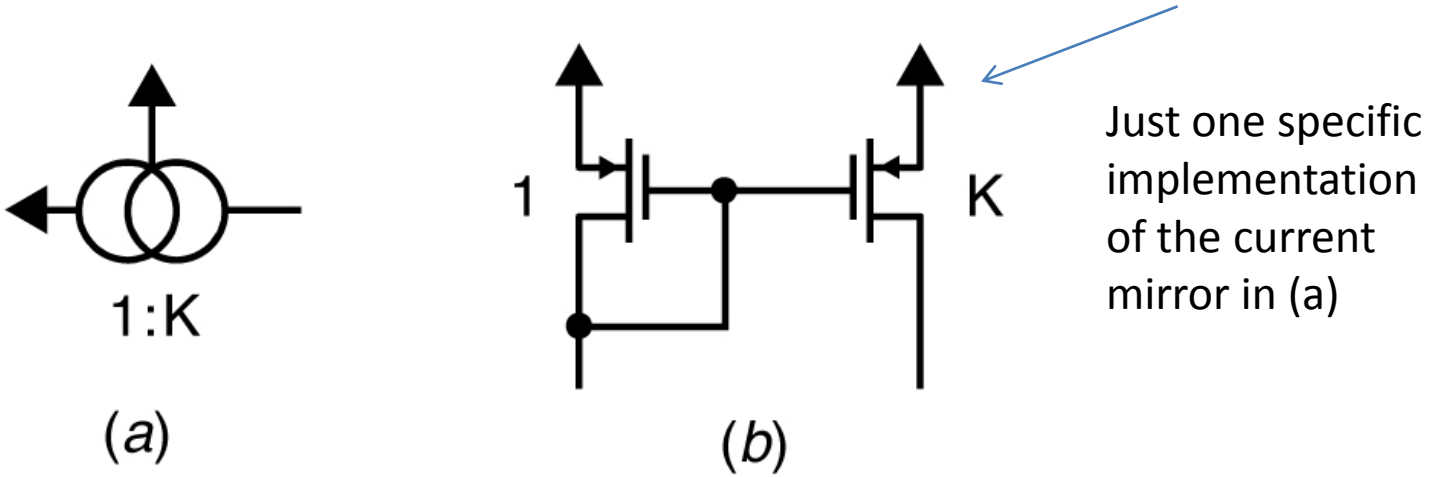
6.3.4 Summary of improved current mirrors

When using the OpAmp-enhanced current mirrors, it may be necessary to add local compensation capacitors to the enhancement loops to prevent ringing during transients.

Also, the settling time may be increased (to tradeoff with large gain).

Many other current mirrors exist, each having its own advantages and disadvantages. Which one to use depends on the requirements of the specific application.

OpAmps may be designed using any of the current mirrors, therefore we can use the following symbol without showing the specific implementation of the current mirror.



Chapter 6 Figure 18

6.4 Folded-cascode OpAmp

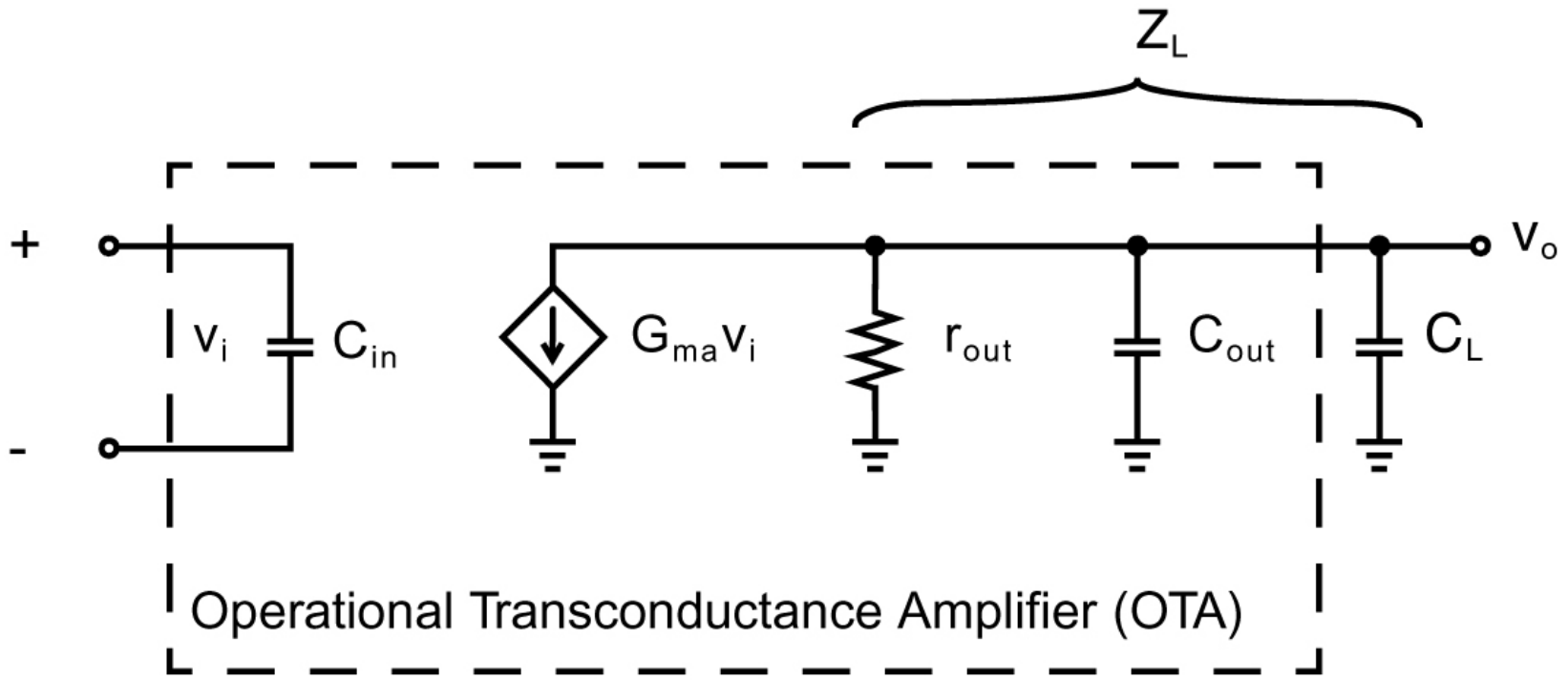
Many modern OpAmps are designed to drive only capacitive loads. In this case, it is not necessary to use a voltage buffer to obtain a low output impedance. So it is possible to realize OpAmps with higher speeds and larger signal swings than those that drive resistive loads.

These OpAmps are possible by having only a single high-impedance node at the output. The admittance seen at all other nodes in these OpAmps are on the order of $1/g_m$, and in this way the speed of OpAmp is maximized.

With these OpAmps, compensation is usually achieved by the load capacitance C_L. As C_L gets larger, these OpAmps gets more stable but also slower.

One of the most important parameters of these modern OpAmps is g_m (ratio of output current over input voltage), therefore they are sometimes referred to as Operational Transconductance Amplifiers (OTA).

A simple first order small-signal model for an OTA may be shown below:



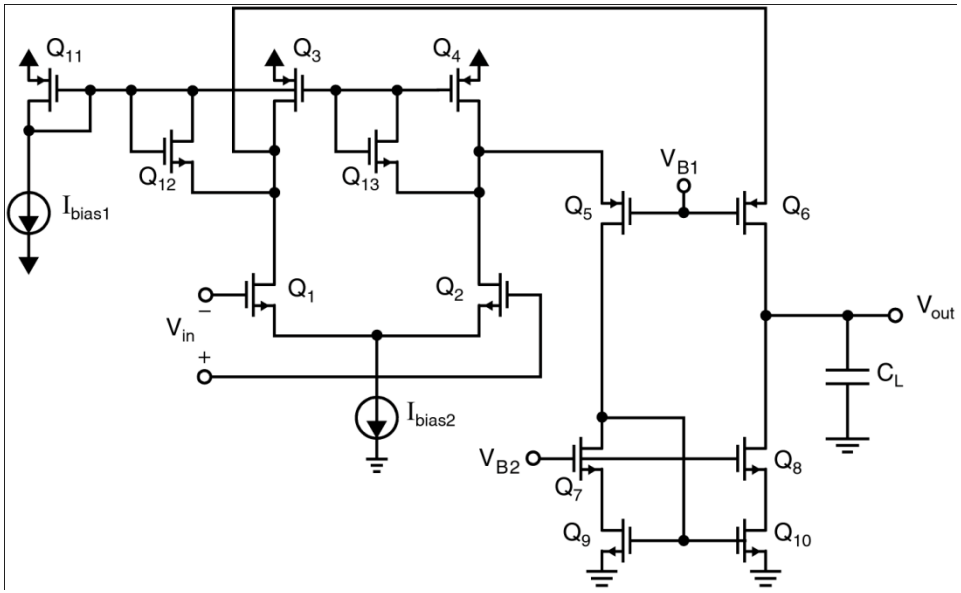
Chapter 6 Figure 19

Folded-cascode OpAmp

A differential-input single-ended output folded-cascode OpAmp is shown below. The current mirror in the output side is a wide-swing cascode one, which increases the gain.

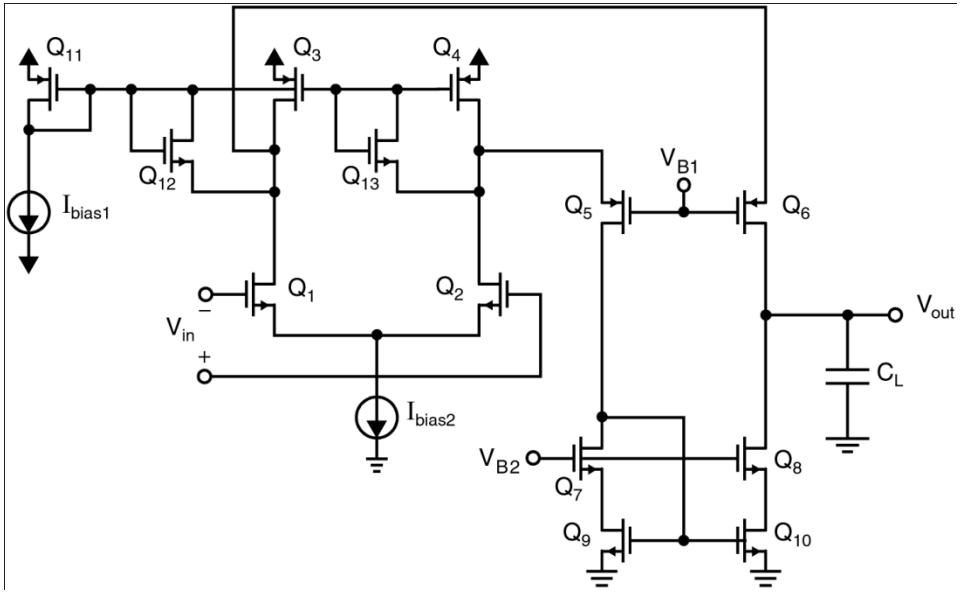
The basic idea of the FC-OpAmp is to apply cascode transistors to the input differential pair but using transistors opposite in type from those used in the input stage. (i.e. Q1, Q2 nMOS and Q5, Q6 pMOS). This arrangement allows the output to be the same as the input bias voltage.

The gain could be large due to large output impedance. If even larger gain is desired, one can use gain-enhancement techniques to Q5-Q8 as described in 6.3.2.



Chapter 6 Figure 20

Folded-cascode OpAmp



Chapter 6 Figure 20

DC biasing: note $I_{D3/4}=I_{D1/2}+I_{D5/6}$

The single-ended output FC-OpAmp can be converted to a fully-differential one (to be detailed later).

A biasing circuit can be included to replace I_{bias1}, I_{bias2} and connect to V_{B1} and V_{B2}.

The two extra transistors Q12 and Q13 can increase slew rate performance and prevent the drain voltages of Q1 and Q2 from having large transients thus allowing the OpAmp to recover faster following a slew rate condition.

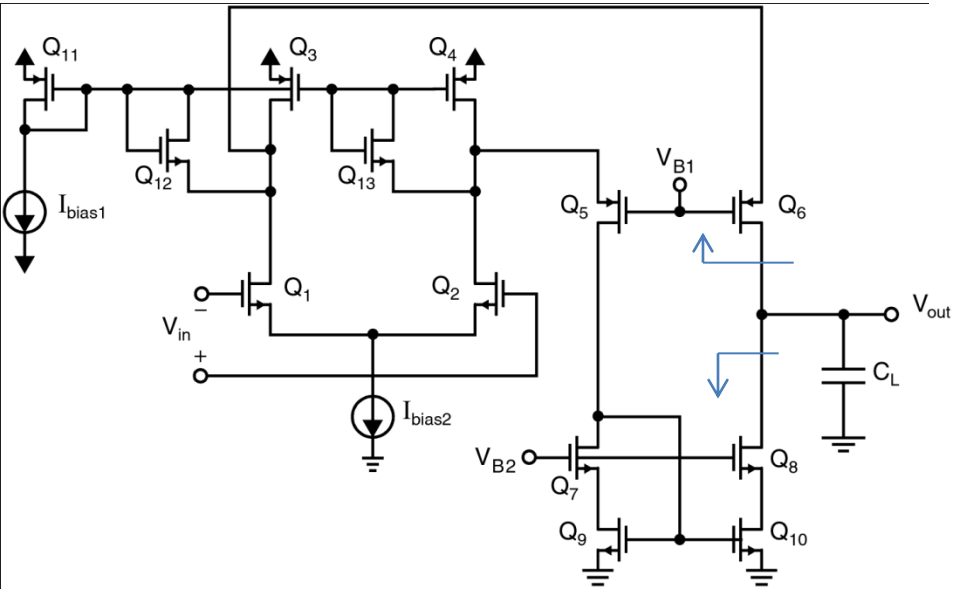
The compensation is realized by the load capacitor C_L (dominant pole compensation). When C_L is small, it may be necessary to add additional capacitors in parallel with the load. If lead compensation is to be used, then a resistor is in series with C_L.

6.4.1 Small-signal analysis

In small-signal analysis, the small-signal current from Q1 goes directly from source to drain and to C_L, while that of Q2 indirectly through Q5 and current mirror of Q7-Q10 to C_L. (assuming $1/g_{m5/6}$ much larger than rds3 and rds4).

Note that these small-signal currents go through different path to the output, therefore their transfer function are different (due to the pole/zero caused by the current mirror for small-signal current of Q2). However, usually, these pole/zero are much larger than the unity-gain frequency of OpAmp and may be ignored.

So an approximate gain transfer function is: $A_V = \frac{V_{out}(s)}{V_{in}(s)} = g_{m1} Z_L(s)$ $A_V = \frac{g_{m1} r_{out}}{1 + s r_{out} C_L}$



Chapter 6 Figure 20

Z_L is the parallel of impedance at drain of Q6, Q8, and C_L.

At high frequencies, Av is approximated as

$$A_V \cong \frac{g_{m1}}{sC_L}$$

unity-gain frequency of the opamp is found to be

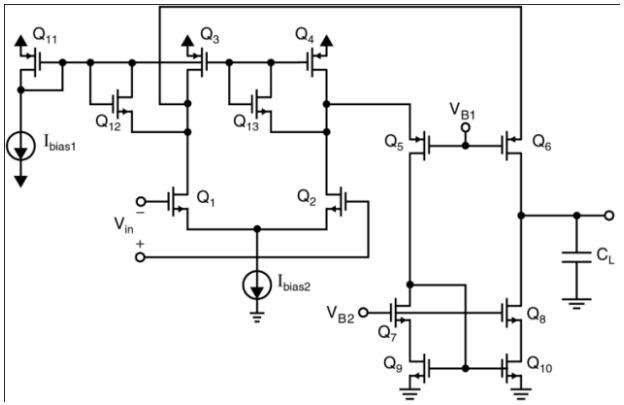
$$\omega_{ta} = \frac{g_{m1}}{C_L}$$

6.4.1 Small-signal analysis

The first-order model shows close to 90 degrees of phase margin.

To maximize bandwidth, it is desirable to increase g_m by using nMOS transistors, which means larger DC current on Q1/2 (Having large g_m for Q1/2 also help reduce noise). Smaller currents on Q5/6 helps increase r_{out}, which increases the DC gain. (the current ratio between them has a practical limit of 4 to 5.)

For more detailed analysis, the second pole is associated with the time constants at the source terminals of Q5/Q6. At high frequencies, the impedance is on the order of $1/g_{m5/6}$, which in this case is relatively large due to smaller current. (so one can have larger currents in order to push this pole away and minimizing the capacitance is important too).



Chapter 6 Figure 20

In summary, if the phase margin of a folded-cascode opamp with feedback is insufficient, one has two choices:

a. Add an additional capacitance in parallel with the load to decrease the dominant pole. This improves phase margin without additional power consumption and without effecting the dc gain, but decreases amplifier bandwidth and increases area.

b. Increase the current and device widths in the output stage, I_{D5} and I_{D6}. This will increase the second pole frequency and improve phase margin, but sacrifices dc gain and increases power consumption.

C. Lead compensation $A_V = \dfrac{g_{m1}}{\dfrac{1}{r_{out}} + \dfrac{1}{R_C + 1/sC_L}} \cong \dfrac{g_{m1}(1 + sR_CC_L)}{sC_L}$

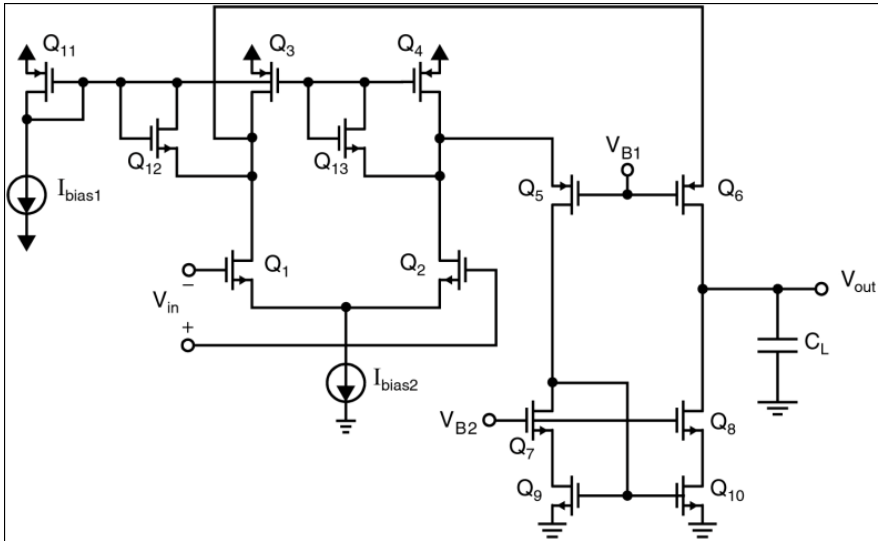
R_C can be chosen to place a zero at 1.7 times the unity-gain frequency.

6.4.2 Slew rate

Diode-connected transistors Q12/13 are turned off during normal operation (as $V_{gd3/4}=V_{gs12}<|V_{tp}|$) and have almost no effect on the OpAmp. However, they improve the operation during slew rate limiting.

If they are not present, then when slew rate occurs, all bias current of Q4 go to Q5 and out of C_L through the mirror (at the same time Q6 conducts zero current in most cases). $SR = \frac{I_{D4}}{C_L}$

At this time, since all I_{bias2} is diverted through Q1 and it is usually larger than I_{D3}, both Q1 and I_{bias2} go into triode region, causing I_{bias2} to decrease until it is equal to I_{D3}. As a result, the drain voltage of Q1 approaches ground. When OpAmp is back to normal operation, drain voltage of Q1 must slew back to the original biasing voltage, and this additional slewing increases distortion and transient delay.



Chapter 6 Figure 20

If Q12/13 were included, then when slew rate occurs (as the above case), Q12 conducts extra current from Q11 and also the current on Q3/4 increases, which eventually makes the sum of I_{D12} and I_{D3} equal to I_{bias2}. On the other hand, $I_{D3/4}$ increment also make the slew rate larger.

Example 6.9 (page 272)

Find reasonable transistor sizes for the folded-cascode opamp shown in Fig. 6.20 to satisfy the following design parameters. Also find the opamp's unity-gain frequency (without feedback) and slew rate, both without and with the clamp transistors.

- Assume the process parameters for the 0.18-µm process in Table 1.5, a single 1.8-V power supply, and limit the current dissipation of the opamp to 0.4 mA.
- Set the ratio of the current in the input transistors to that of the cascode transistors to be 4:1. Also, set the bias current of Q_{11} to be 1/10th that of Q_3 (or Q_4) such that its current can be ignored in the power dissipation calculation.
- The maximum transistor width should be 180 µm and channel lengths of 0.4 µm should be used in all transistors.
- All transistors should have effective gate-source voltages of around 0.24 V except for the input transistors, whose widths should be set to the maximum value of 180 µm. Also, round all transistor widths to the closest multiple of 2 µm, keeping in mind that if a larger transistor is to be matched to a smaller one, the larger transistor should be built as a parallel combination of smaller transistors.
- Finally, assume the load capacitance is given by $C_L = 2.5$ pF.

$$I_{total} = I_{D3} + I_{D4} = 2(I_{D1} + I_{D6}) = 2(4I_B + I_B) = 10I_B \longrightarrow I_B = I_{D5} = I_{D6} = \frac{I_{total}}{10} = 40\ \mu A$$

$$I_{D3} = I_{D4} = 5I_{D5} = 200\ \mu A \quad I_{D1} = I_{D2} = 4I_{D5} = 160\ \mu A$$

all transistor channel lengths be 0.4 µm

This choice allows us to immediately determine the sizes of most transistors using $\left(\frac{W}{L}\right)_i = \frac{2I_{Di}}{\mu_i C_{ox} V_{effi}^2}$

Q_1	180/0.4	Q_6	8/0.4	Q_{11}	4/0.4
Q_2	180/0.4	Q_7	2/0.4	Q_{12}	4/0.4
Q_3	40/0.4	Q_8	2/0.4	Q_{13}	4/0.4
Q_4	40/0.4	Q_9	2/0.4		
Q_5	8/0.4	Q_{10}	2/0.4		

Derived from Q3/4

Pre-set to maximum in order to maximize g_m

Arbitrarily set equal to Q11

the transconductance of the input transistors would be given by

$$\sqrt{2I_{D1}\mu_n C_{ox}(W/L)_1} = 6.24 \text{ mA/V}$$

$$\omega_{ta} = \frac{g_{m1}}{C_L} = 1.6\times10^9 \text{ rad/s} \Rightarrow f_{ta} = 255 \text{ MHz}$$

The slew rate without the clamp transistors is given by

$$SR = \frac{I_{D4}}{C_L} = 80 \text{ V/}\mu\text{s}$$

When the clamp transistors are included, during slew-rate limiting, we have

$$I_{D12} + I_{D3} = I_{bias2}$$
$$I_{D3} = 10I_{D11}$$
$$I_{D11} = 20\ \mu\text{A} + I_{D12}$$

$$\Rightarrow I_{D11} = \frac{I_{bias2} + 20\ \mu\text{A}}{11} = 30.9\ \mu\text{A}$$

$$I_{D3} = I_{D4} = 10I_{D11} = 0.309 \text{ mA}$$

$$SR = \frac{I_{D4}}{C_L} = 124 \text{ V/}\mu\text{s}$$

Example 6.10 (page 274)

The opamp in Example 6.9 is simulated and found to have an equivalent second pole frequency at $\omega_{eq} = 2\pi \cdot 365$ MHz. Select a value for the lead compensation resistor, R_C, to provide a phase margin of 85° when the opamp is used in a unity-gain configuration.

Solution

The phase margin without R_C is given by

$$\text{Phase Margin} = 90° - \tan^{-1}\left(\frac{\omega_t}{\omega_{eq}}\right) = 90° - \tan^{-1}\left(\frac{2\pi \cdot 255\ \text{MHz}}{2\pi \cdot 365\ \text{MHz}}\right) = 55°$$

In order to increase this by $30° = \tan^{-1}(1/1.7)$, the lead compensation zero must be placed at $1/R_C C_L = 1.7\omega_t$. Since $\beta = 1$, we have $\omega_t = \omega_{ta}$. Hence, a reasonable size for R_C in series with C_L is given by

$$R_C = \frac{1}{1.7 C_L \omega_t} = \frac{1}{1.7 g_{m1}} = 147\ \Omega \qquad (6.118)$$