

Digital Integrated Circuits A Design Perspective

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The Inverter

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Propagation Delay

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CMOS Inverter Propagation Delay



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MOS transistor model for simulation



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Computing the Capacitances

Consider each capacitor individually is almost impossible for manual analysis. What capacitors count in C_{L} ?



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Computing the Capacitances

□ NMOS and PMOS transistor are either in cutoff or saturation mode during at least the first half (50%) of the output transient.

□ So, the only contributions to C_{gd} are the overlap capacitance, since channel capacitance occurs between either Gate-Body for transistors in cutoff region or Gate-Source for transistors in saturation region.

The Miller Effect

The lumped capacitor model requires the floating C_{gd1} capacitor be replaced by a capacitor to GND using Miller effect.



"A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value."

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Consider the situation that an impedance is connected between *input* and *output* of an amplifier



- The same current flows from (out) the top input terminal if an impedance $Z_{in,Miller}$ is connected across the input terminals
- The same current flows to (in) the top output terminal if an impedance $Z_{out,Miller}$ is connected across the output terminal
- ➤ This is know as Miller Effect
- Two important notes to apply Miller Effect:
 - \checkmark There should be a common terminal for input and output
 - ✓ The gain in the Miller Effect is the gain after connecting feedback impedance Z_f

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Inverter Graphs from Prentice Hall

Computing the Capacitances

Capacitor	Expression
C_{gd1}	2 CGD0 W _n
C_{gd2}	2 CGD0 W _p
C _{db1}	$K_{eqn} (AD_n CJ + PD_n CJSW)$
C _{db2}	$K_{eqp} (AD_p CJ + PD_p CJSW)$
C _{g3}	C _{ox} W _n L _n
C _{g4}	C _{ox} W _p L _p
C _w	From Extraction
C_L	Σ

The capacitance between drain and bulk, C_{db1} and C_{db2} , are due to the reverse-biased pn-junction.

Such a capacitor is, unfortunately, quite nonlinear and depends heavily on the applied voltage.

In Chapter 3 we replaced the nonlinear capacitor by a linear one with the same change in charge for the voltage range of interest. A multiplication factor, K_{eq} , is introduced to relate the linearized capacitor to the value of the junction capacitance under zero-bias conditions (usually in the range of 0.6 to 0.9).

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Junction Capacitance



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Linearizing the Junction Capacitance

Replace non-linear capacitance by large-signal equivalent linear capacitance which displaces equal charge over voltage swing of interest

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq}C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1 - m)} [(\phi_0 - V_{high})^{1 - m} - (\phi_0 - V_{low})^{1 - m}]$$

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Table 6: Contact to Active

Rule	Description	Lambda
6.1	Exact contact size	2 x 2
6.2	Minimum active overlap	1.5
6.3	Minimum contact spacing	3
6.4	Minimum spacing to gate of transistor	2







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Junction Capacitance Ls (from Ch. 3)



Computation of all capacitors

	C_{ox} (fF/ μ m ²)	С _О (fF/µm)	C_j (fF/ μ m ²)	<i>m</i> _j	$egin{array}{c} \phi_b \ (V) \end{array}$	C _{jsw} (fF/µm)	m _{jsw}	$egin{array}{c} \phi_{bsw} \ (\mathcal{V}) \end{array}$
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Table 5.2 Components of C_L (for high-to-low and low-to-high transitions).

	Value (fF) (L→H)	Value (fF) (H→L)	Expression	Capacitor
	0.23	0.23	2 CGD0 _n W _n	C _{gd1}
Intrinsic	0.61	0.61	$2 \text{ CGD0}_{p} \text{ W}_{p}$	C _{gd2}
	0.90	0.66	$\mathrm{K}_{\mathrm{eqn}}\mathrm{AD}_{\mathrm{n}}\mathrm{CJ}+\mathrm{K}_{\mathrm{eqswn}}\mathrm{PD}_{\mathrm{n}}\mathrm{CJSW}$	C _{db1}
	1.15	1.5	$K_{eqp} AD_p CJ + K_{eqswp} PD_p CJSW$	C _{db2}
ovtrinsic	0.76	0.76	$(CGD0_n + CGSO_n) W_n + C_{ox} W_n L_n$	C _{g3}
	2.28	2.28	$(CGD0_p+CGSO_p) W_p + C_{ox} W_p L_p$	C _{g4}
	0.12	0.12	From Extraction	<i>C</i> _w
	6.0	6.1	Σ	C_L

C_{db} will be **slightly** different (the pn junction reverse bias in L-to-H and H-to-L, why? voltage range) © Digital Integrated Circuits^{2nd} Inverter

Transient Response

 C_{gd} directly couples the steep input change before the circuit can even start to react to the changes at input (potential forward bias the pn junction)



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Low-to-High and High-to-Low delay

□ It is desired to have identical propagation delays for both rising and falling inputs.

Equal delay requires equal equivalent onresistance, thus equal current IDAST (neglecting the channel length modulation)

□ This demands almost the same requirements for a V_m at V_{DD}/2. Why?

Requirements for equal delay

$$I_{DSAT} = k' \frac{W}{L} \left((V_{DD} - V_T) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right)$$
$$I_{Dn} = k_n' \left(\frac{W}{L} \right)_n V_{DSATn} \left((V_{DD} - V_{Tn}) - \frac{V_{DSATn}}{2} \right)$$
$$I_{Dp} = k_p' \left(\frac{W}{L} \right)_p V_{DSATp} \left((V_{DD} - V_{Tp}) - \frac{V_{DSATp}}{2} \right)$$

Assume
$$V_{DD} >> V_{Tp} + V_{DSATp} / 2$$

then $\frac{k_p V_{DSATp} (W/L)_p}{k_n V_{DSATn} (W/L)_n} = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = 1$

This is exactly the formerly defined parameter r (last lecture)

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Design for delay performance Keep capacitances small careful layout, e.g. to keep drain diffusion as small as possible

Increase transistor sizes watch out for self-loading! When intrinsic capacitance starts to dominate the extrinsic ones

Increase VDD (????)

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Delay as a function of V_{DD}



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Device Sizing



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NMOS/PMOS ratio



Widening PMOS improves the L-H delay by increasing the charge current, but it also degrades the H-L by giving a larger parasitic capacitance. Considering average is more meaningful!!

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Delay Definitions



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Impact of Rise Time on Delay



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Custom design process: An inverter design example

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1. Schematic design



2. Layout design

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Inverter

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Step 1: define Nwell (for PMOS)

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Step 2: define pselect (for PMOS location)

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Step 3: define active region (for PMOS)

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Step 5: define contacts (for PMOS)

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Step 6: define Vdd and connect source (of PMOS) to it

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Step 7: make at least one Nwell contact

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Step 8: create NMOS (repeat similar steps before except you do not need make Nwell)

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step9: make input and output connections

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2. DRC (Design Rule Check)

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Correct error if there is any



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3. LVS (Layout versus Schematic)

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4. Extract Layout parasitics and post-layout simulation



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CMOS Inverter





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Two Inverters

Layout preference: *Share power and ground Abut cells*





Impact of Process Variations (DFM)



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Inverter Sizing for delay

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Inverter with Load

W means the size is increased by a factor of *W* with respect to the minimum size



 $\begin{aligned} \text{Delay} &= kR_W(C_{int} + C_L) = kR_WC_{int} + kR_WC_L \\ &= \text{Delay (Internal)} + \text{Delay (Load)} \\ &= kR_WC_{int}(1 + C_L/C_{int}) \end{aligned}$

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Delay as function of size

$$Delay = kR_W C_{int}(1 + C_L / C_{int})$$

= Delay (Internal) + Delay (Load)

$$R_{w} = R_{unit} / W; C_{int} = W C_{unit}$$
$$t_{p} = t_{p0} (1 + C_{L} / (W C_{unit}))$$
$$t_{p0} = 0.69 R_{unit} C_{unit}$$

• Intrinsic delay is fixed and independent of sizeW

• Making *W* large yields better performance gain, eliminating the impact of external load and reducing the delay to intrinsic only. But smaller gain at penalty of silicon area if *W* is too large!

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$$Delay \sim R_W (C_{int} + C_L)$$

$$t_p = kR_W C_{int} (1 + C_L / C_{int}) = t_{p0} (1 + f / \gamma)$$

 $C_{int} = \gamma C_{gin}$ with $\gamma \approx 1$ for modern technology (see page199 in book or Slid 14 for an example) C_{gin} : input gate capacitance

 $C_L = f C_{gin}$ - effective fanout This formula maps the intrinsic capacitor and load capacitor as functions of *a common capacitor*, which is the gate capacitance of the minimum-size inverter

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Single inverter versus inverter chain

Gate sizing for an isolated gate is not really meaningful. Realistic chips always have a long chain of gates.

□ So, a more relevant and realistic problem is to determine the optimal sizing for a chain of gates.

Inverter Chain



If C_L is given:

- How many stages are needed to minimize the delay?
- How to size the inverters?

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Apply to Inverter Chain (fixed N stages)

Unit size (minimum size) inverter



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Optimal Tapering for Given N

 \Box Delay equation has *N* - 1 unknowns, $C_{gin,2} - C_{gin,N}$

 \Box Minimize the delay, find N - 1 partial derivatives equated to 0

D Result:
$$C_{gin,j+1}/C_{gin,j} = C_{gin,j}/C_{gin,j-1}$$

□ Size of each stage is the geometric mean of two neighbors

$$C_{gin,j} = \sqrt{C_{gin,j-1}C_{gin,j+1}}$$

- each stage has the same effective fanout
- each stage has the same delay

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Optimum Delay for fixed N stages

When each stage is sized by *f* and has same effective fanout *f*:

$$f^N = F = C_L / C_{gin,1}$$
 effective fanout
of the overall

circuit

Effective fanout of each stage:

$$f = \sqrt[N]{F}$$

Minimum path delay

$$t_{p} = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{i=1}^{N} \left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}} \right) = N t_{p0} \left(1 + \sqrt[N]{F} / \gamma \right)$$

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 C_L/C_1 has to be evenly distributed across N = 3 stages:

$$f = \sqrt[3]{8} = 2$$

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Optimum Number of Stages

For a given load C_L and given input capacitance C_{in} Find optimal sizing f

$$C_{L} = F \cdot C_{in} = f^{N}C_{in} \text{ with } N = \frac{\ln F}{\ln f}$$

$$t_{p} = Nt_{p0} \left(F^{1/N} / \gamma + 1\right) = \frac{t_{p0} \ln F}{\gamma} \left(\frac{f}{\ln f} + \frac{\gamma}{\ln f}\right)$$

$$\frac{\partial t_{p}}{\partial f} = \frac{t_{p0} \ln F}{\gamma} \cdot \frac{\ln f - 1 - \gamma / f}{\ln^{2} f} = 0$$
For $\gamma = 0, f = e, N = \ln F$

$$f = \exp(1 + \gamma / f)$$

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Optimum Effective Fanout f Optimum f for given process defined by γ $f = \exp(1 + \gamma/f)$ $f_{opt} = 3.6$ for $\gamma = 1$



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Impact of introducing buffers

$$t_p = N t_{p0} \left(1 + \sqrt[N]{F} / \gamma \right) \qquad f_{opt} = 4$$

F	Unbuffered	Two Stage	Inverter Chain
10	11	8.3	8.3
100	101	22	16.5
1000	1001	65	24.8
10,000	10,001	202	33.1

Buffer Design



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Intel Itanium Microprocessor



1000um

Itanium has 6 integer execution units like this

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