MINLP Based Topology Synthesis for Delta Sigma Modulators Optimized for Signal Path Complexity, Sensitivity and Power Consumption

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Abstract

This paper proposes a novel architecture synthesis algorithm for single-loop single-bit $\Delta\Sigma$ modulators. We defined a generic modulator architecture and derived its noise and signal transfer function (NTF/STF) in symbolic forms. We then used the TF in MINLP to generate optimal topologies for a variety of design requirement, such as modulator complexity, sensitivity and power consumption, which appeard as cost functions. Experiments show the superiority of synthesized topologies as compared to traditional solutions.

1. Introduction

Because of its promise to deliver short design closure at much lesser costs, high-level synthesis (HLS) is rapidly becoming a main topic in today's system-on-chip (SoC) design [1, 3, 8, 15]. Though HLS is well defined for digital circuits, there is a lack of systematic system design methodologies for analog and mixed-signal circuits, which are essential components of any modern SoC. Current research on analog and mixed-signal CAD mostly addresses transistor sizing and layout generation, which are activities at low level of abstraction [8]. Analog and mixed-signal high-level synthesis (AMS-HLS) consists of four main tasks [1, 3, 4, 8]: (i) system specification, (ii) architecture synthesis (architecture generation and selection), (iii) constraint transformation, and (iv) design verification. High level activities, such as exploring for feasible system topologies and optimizing their parameters, are critical to developing constraint-satisfying or optimal system design [3, 8].

Inspite of their importance, AMS high-level activities remain purely manual, being accessible only to a small number of expert analog designers. In real-life, mixed-signal designers may have a library of popular architectures to choose from. Then, architectures are selected from the library based on the designer's experience. This is obviously an expensive and lengthy process that does not guarantee any optimality for the selected architecture. Recently, several methods were attempted to tackle the very challenging problem of automatically generating and selecting optimal topologies. Doboli and Vemuri [3] present an architecture generation and selection technique based on tabu search exploration guided by the signal flow graph of a system. Antao and Brodersen [1] use the state-space equations of a filter to create different signal flow graphs, which are then used (through a mapping process) to create filter implementations. In spite of their novelty, these methods cannot be used for automatically synthesizing topologies for more complex systems, like $\Delta\Sigma$ modulators.

In this paper, we presented an original method for systematically and automatically generating architectures for single-loop single-bit $\Delta\Sigma$ modulators. These modulators are important components of many mixed-signal SoC. The crux of the synthesis method is a generic representation that describes all possible modulator topologies. The symbolic expressions for Noise Transfer Function (NTF) [12] and Signal Transfer Function (STF) [12] were derived for the generic topology. A MINLP (Mixed Integer Nonlinearly Constrained Programming) description was formulated to simultaneously generate and select the best topology under various design requirements, such as system hardware complexity, sensitivity under parameter variation, and power consumption. Experiments for 3^{rd} and 4^{th} order $\Delta\Sigma$ modulators showed that the synthesized topologies are significantly superior to traditional topologies.

We assumed that the topology for a single-loop, single-bit $\Delta\Sigma$ modulator is a signal flow graph containing integrators and having all its signal paths and coefficients of the signal paths defined, so that it realizes a desired TF (NTF and STF). Hence, a modulator topology differs from another one in terms of (1) the type of their integrators (delayed or delayless integrators), (2) their signal paths (whether they have the same signal paths or not), and (3) the numerical coefficients of their signal paths. For AMS-HLS, the three categories define the control parameters for topology synthesis, as they uniquely determine a topology. Then, generating optimal $\Delta\Sigma$ modulator topologies is equivalent to having *all* control parameters as unknowns and solving for their values that optimize certain performance criteria,

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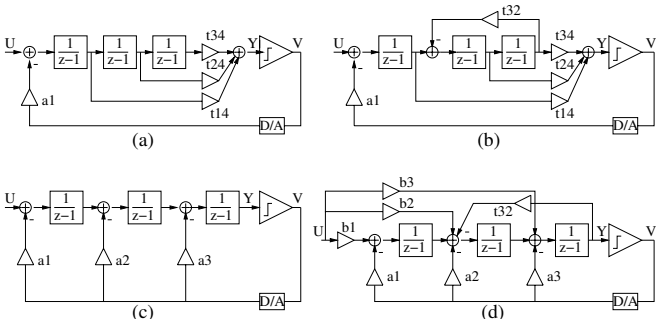

Figure 1: 3^{rd} order $\Delta\Sigma$ modulator topologies

such as SNR, DR, system complexity, sensitivity, and power consumption.

This paper is organized as follows. Section 2 reviews similar work. Section 3 presents the generic topology for $\Delta\Sigma$ modulator and the related TF. Section 4 discusses MINLP formulation for obtaining optimal ADC topologies. Experiments are offered in Section 5. Finally, conclusions are provided.

2. Previous work on $\Delta\Sigma$ modulator synthesis

The related literature presents several ways of exploring for possible $\Sigma\Delta$ modulator topologies. One way is to pre-set the integrator types and signal paths, and explore only for the coefficient values [10, 14]. By setting the first two types of control parameters, a set of incomplete topologies is defined. Several types of incomplete topologies are quite popular for different orders of single-bit, single-loop $\Delta\Sigma$ modulator [5, 9, 12, 13]. Figure 1 depicts some well-known topologies for 3^{rd} order $\Delta\Sigma$ modulator. In this methodology, designers first decide with regard to which of the incomplete topologies should be used. Then, coefficients of the chosen topology are calculated for the desired TF, thus completing the process of topology design [10, 11, 14]. As it can be noticed, there is no scheme to get an optimal topology. Designers have to select an incomplete topology based on their experience. One straightforward way to improve this methodology is to let designers try out all pre-selected topologies and then decide which one is optimal. The methodology implemented in DAISY [7] follows this idea. A similar concept is also suggested by Bajdechi *et al* [2]. Given the design specification, e.g., SNR and DR, the tool selects one from a set of topologies with the smallest power consumption.

The main limitation of existing synthesis techniques is that most of the topology control parameters (integrator types, signal paths, and coefficient values) are pre-set, which severely restricts the solution space for topology generation. As a result, solutions are actually representing only local optima for a given set of requirements. To find the real mathematical optima, all control parameters ought to be considered. This paper proposes a MINLP based topology synthesis method that considers all control variables as unknowns, and is capable of finding mathematical optima through solving mixed-integer nonlinear equations.

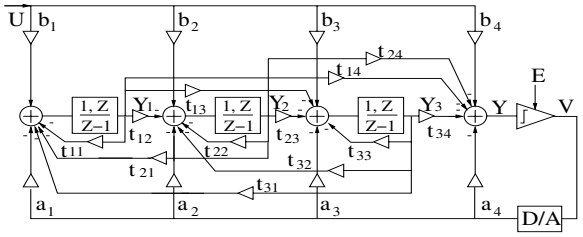

Figure 2: Generic 3^{rd} order $\Delta\Sigma$ topology

3. Generic topology for $\Delta\Sigma$ modulators

The crux of the proposed topology synthesis method is a generic representation that describes all possible topologies for single-bit single-loop $\Delta\Sigma$ modulators. Figure 2 shows the representation for 3^{rd} order $\Delta\Sigma$ modulators, but similar representations exist for higher order modulators also.

The generic representation includes all possible feedback and feedforward signal paths. Y_i represents the output of the i^{th} integrator, and Y is the input to the quantizer. A_i stand for the feedback coefficients from the output to the i^{th} adder, b_i are the feedforward coefficients from the input to the i^{th} adder, and t_{ji} are the coefficients from Y_j to the i^{th} adder in the modulator. There are negative signs for all t_{ji} and a_i coefficients. Please note that some of the signal paths in the generic topology may seem redundant to expert designers: for example, in Figure 2, signal path with design coefficient a_4 never exists in the generated topology. However, for the sake of completeness, these paths were also considered.

Let N be the modulator order. Then, following expressions hold as a general rule:

$$t_{ji} \geq 0, if\ j \geq i, j = 1, ...N, i = 1, ...N+1$$
$$t_{ji} \leq 0, if\ j < i, j = 1, ...N, i = 1, ...N+1$$
$$a_i \geq 0, b_i \geq 0, i = 1, ...N+1 \quad (1)$$

There are $(N+1)\times(N+2)$ coefficients in the generic topology. It can be seen that all "classic" topologies in Figure 1 can be derived from the generic topology by removing some of the signal paths. Note also that integrators could be either delayed or delayless.

For the generic topology, we derived its NTF and STF in terms of the coefficients of all signal paths. We assumed that the quantization noise E is additive white-noise [12]. By generalizing, we calculated symbolic expressions for NTF and STF of single-bit single-loop $\Delta\Sigma$ modulators of any order.

Lemma: Numerator (NTF_n) and denominator (NTF_d) of NTF of $\Delta\Sigma$ modulator of order N are expressed as:

$$NTF_n = \sum_{K=0}^{N}(-1)^{K+1}\left(C_N^K - C_{N-1}^{K-1}\sum_{i=1}^{N} t_{ii} + .. + (-1)^K C_{N-K}^{K-K}\right.$$
$$\left.\sum_{i_1\neq}^{N}\sum_{i_2\neq}^{N}..\sum_{i_K}^{N} t_{i_1(i_1,i_2,..i_K)}t_{i_2(i_1,i_2,..i_K)}t_{i_K(i_1,i_2,..i_K)}\right)z^{N-K}$$

$$NTF_d = \sum_{K=0}^{N}\left((-1)^{K+1}\left(C_N^k - C_{N-1}^{K-1}\sum_{i=1}^{N} t_{ii} + .. + (-1)^K C_{N-K}^{K-K}\right.\right.$$
$$\left.\left.\sum_{i_1\neq}^{N}\sum_{i_2\neq}^{N}..\sum_{i_K}^{N} t_{i_1(i_1,i_2,..i_K)}t_{i_2(i_1,i_2,..i_K)}t_{i_K(i_1,i_2,..i_K)}\right)\right) +$$
$$(-1)^{K+1}\left(C_{N-1}^{K-1}\sum_{i=1}^{N} a_i t_{i,N+1} + C_{N-2}^{K-2}\sum_{i=1}^{N} a_i \sum_{j_1\neq}^{N}\sum_{j_2}^{N}\right.$$

$t_{j_1(N+1,j_2)} t_{j_2(N+1,j_2)} + .. + C_{N-K}^{K-K} \sum_{i=1}^{N} a_i \sum_{j_1 \neq}^{N} \sum_{j_2 \neq}^{N} .. \sum_{j_K}^{N}$
$t_{j_1(N+1,j_2,..j_K)} t_{j_2(N+1,j_2,..j_K)} .. t_{j_k(N+1,j_2,..j_K)} \Big) + a_{N+1}(-1)^{K+1}$
$\Big(C_N^K - C_{N-1}^{K-1} \sum_{i=1}^{N} t_{ii} + .. + (-1)^K C_{N-K}^{K-K} \sum_{i_1 \neq}^{N} \sum_{i_2 \neq}^{N} .. \sum_{i_K}^{N}$
$t_{i_1(i_1,i_2,..i_K)} t_{i_2(i_1,i_2,..i_K)} t_{i_K(i_1,i_2,..i_K)} \Big) \Big) z^{N-K}$

In the above expression, $(i_1, i_2, ..i_K)$ means selecting only one of the them, similarly for $(N+1, j_2, ..j_K)$.

4. Optimal topology generation using MINLP

4.1. MINLP problem formulation

By equating the symbolic TF to the desired TF (desired STF is assumed to be 1), $3 \times (N+1)$ equations are obtained. Obviously, there are an infinite number of solutions considering that the number of unknowns - $(N+1) \times (N+2)$, is always larger than the number of equations - $3 \times (N+1)$.

After carefully analyzing the symbolic expression for NTF and STF, we found following interesting properties: (i) all terms in the expression are nonlinear equations of the defined coefficient variables and (ii) there are no quadratic terms for any of the coefficients. As a result, this formulation is suitable to be solved by Nonlinear Programming (NLP) [6]. Also, in order to select any signal path in the generic topology, a corresponding binary 0/1 variable was defined to denote whether the signal path is present or not.

For a given a cost function f, we formulated the topology synthesis problem as:

$$\begin{gathered} minimize\ cost\ f(x_i, wx_i); \\ subject\ to: g(x_i) = 0; \\ subject\ to: h(x_i, wx_i) \leq 0; \\ subject\ to: x_i\ satisfy\ (1), wx_i \in \{0,1\}; \end{gathered}$$

where x_i denotes any of the unknown coefficients a_i, b_i and t_{ji} defined in (1), g are the $3 \times (N+1)$ equality constraints obtained from equating the symbolic NTF and STF to the desired NTF and STF, and h are the inequality constraints relating the coefficient variables to the binary variables, so that wx_i correclty identify whether the signal path with coefficient x_i is present or not.

The resulting problem can be optimally solved using mixed-integer nonlinear programming (MINLP) [6]. Thus, MINLP solving offers the best topology with respect to the cost function f. MINLP formulation is scalable, and it is easy to add additional constraints.

4.2. Different cost function formulation

Cost function formulation is an important issue for optimal topology synthesis. The proposed method supports three types of cost functions: (1) for minimizing the signal path (hardware) complexity of $\Delta\Sigma$ modulator, (2) for minimizing the sensitivity of the modulator with respect to coefficient variations, and (3) for minimizing the power consumption. These functions are discussed next.

A. Signal path minimization. Since binary variables denote whether the corresponding signal paths are present or not, the cost function f was formulated as:

$$Minimize \sum_{i=1}^{(N+1)(N+2)} wx_i$$

B. Sensitivity minimization. This function considers the total sensitivity of the $\Delta\Sigma$ modulator with respect to variations of the coefficient variables. This optimization is very useful, since process and mismatch induced variations are expected to shift coefficient values away from their nominal values. Minimizing the total sensitivity results in a more stable modulator, and thus improves yield.

Suppose NTF is

$$T(z) = \frac{NTF_n}{NTF_d} = \frac{p_1 z^N + p_2 z^{N-1} + ... + p_{N-1} z + p_N}{q_1 z^N + q_2 z^{N-1} + ... + q_{N-1} z + q_N}$$

Then, the cost function f could be written as:

$$Minimize(\sum_{i=1}^{(N+1)(N+2)} \sum_{j=1}^{N} \frac{\delta p_j}{\delta x_i} + \sum_{i=1}^{(N+1)(N+2)} \sum_{k=1}^{N} \frac{\delta q_k}{\delta x_i})^2$$

The sensitivity value was squared to encourage getting a value close to zero (corresponding to no sensitivity with respect to small variations of the coefficient variables).

The calculation of the sensitivity function $\frac{\delta p_j}{\delta x_i}$ and $\frac{\delta q_k}{\delta x_i}$ is quite easy, since we already derived the symbolic expressions for NTF. Each of the coefficients for NTF was symbolically calculated too. Note that STF could be part of the cost function too.

C. Power consumption minimization. We used a power consumption estimation method based on the work by Medeiro *et al* [11]. For a switch-capacitor circuit implementation of the modulator, the power consumption mainly consist of static power consumption of OpAmp circuits, and dynamic power consumption of capacitors. Static power consumption can be approximated as $P_s = I_{bias} V_{supply} N$, where V_{supply} is the supply voltage and N represents the order of the modulator. To minimize static power consumption, we need to minimize I_{bias}, which comes down to minimize C_{eq}, the equivalent load for the input integrator [11]. For example, for the generic topology in Figure 2, $C_{eq} = C_s(1 + \beta + \frac{a_1}{b_1} + \frac{t_{11}}{b_1} + \frac{t_{21}}{b_1} + \frac{t_{31}}{b_1} + \alpha + \alpha(b_1 + \beta + a_1 + t_{11} + t_{21} + t_{31}))$, where C_s is the sampling capacitor and parasitic capacitors $C_p = \beta C_s$ and $C_l = \alpha C_s$ $(0 \leq \alpha, \beta \leq 1)$. So, once C_s is set from thermal noise consideration [11], C_{eq} satisfy $C_{eq} = KC_s$, where $K \in R$. Dynamic power consumption is dissipated to charge a capacitor of value C at frequency of f_s between reference voltages V_r. It can be estimated as $P_d = (2V_r)^2 C f_s$ (considering fully differential circuitry). To minimize it, we need to minimize the total capacitance of the modulator. Similar to the way of deriving C_{eq}, C_{total} was formulated as $C_{total} = C_s((1 + \frac{1}{b_1} + \frac{a_1}{b_1} + \sum_{j=1}^{N} \frac{t_{j1}}{b_1}) +$

$\sum_{i=2}^{N}(1+\frac{1}{t_{(i-1)(i)}}+\frac{a_i}{t_{(i-1)(i)}}+\frac{b_i}{t_{(i-1)(i)}}+\sum_{j\neq(i-1)}^{N}\frac{t_{ji}}{t_{(i-1)(i)}})$
$+(1+\frac{a_{N+1}}{t_{(N)(N+1)}}+\frac{b_{N+1}}{t_{(N)(N+1)}}+\sum_{j\neq N}^{N}\frac{t_{(j)N+1}}{t_{(N)(N+1)}})).$

4.3. Topology exploration flow

The proposed topology synthesis flow for $\Delta\Sigma$ modulators is shown in Figure 3. The inputs to the flow are design specifications, such as desired SNR, and DR. Based on the desired performance, an initial order N_{init} of the $\Delta\Sigma$ modulator is estimated ($1 \leq N \leq 8$). Also, two additional design parameters are considered, the Oversampling Ratio (OSR) and maximum NTF magnitude (MAG). These two design parameters are confined within certain ranges, and initially set to their minimal values. For example, OSR_{init} can be set to 16 ($16 \leq OSR \leq 256$), and MAG_{init} to 1.2 ($1.2 \leq MAG \leq 2.0$ according to Lee's rule [14]).

Next, the method sets the type for each of the integrators in the modulator. This has to be done first, because different combinations of integrator types lead to different symbolic expression for NTF and STF. There maybe a large number of combinations of integrator types for an N_{th} order $\Delta\Sigma$ modulator, considering that each integrator can be either of delayed or delayless type. Theoretically the total number of combinations is 2^N. In theory, to obtain the optimal topology, all these combinations should be considered. In our flow, we considered a library of combinations of integrator types. Figure 4 shows some combinations of the integrator types for 3^{rd} and 4^{th} order $\Delta\Sigma$ modulators.

After integrator types are set, based on N_{init}, OSR_{init} and MAG_{init}, a NTF is generated similar to [14]. Then, using the symbolic formulas in Section 3, MINLP description is generated, and solved with an NLP solver [6]. The topology obtained after solving the MINLP program is behaviorally simulated to test whether the SNR and DR meet the specification. If yes, an optimal topology is generated for the current combination of integrator types. Otherwise, first it considers increasing MAG until its maximum limit is reached. Then, it considers increasing OSR until its maximum limit is reached, and finally it considers increasing the modulator order until the order is out of range. If an optimal solution is obtained for a combination of minimal MAG and OSR values, the solution is saved as optimal for the current combination of integrator types. If there are some other combinations of integrator types that are not yet explored, the design shifts to another combination, and the process is repeated until all combinations are analyzed.

After this, a set of solutions, each of which is actually a local optima for a particular combination of integrator types, is passed to the final synthesis stage, where it is subject to one or more tests for picking the global optimal solution. For example, if we are using the cost function of minimum total sensitivity, the set of local optima is subject to minimum sensitivity test via Monte-Carlo analysis. The solution with least sensitivity and most

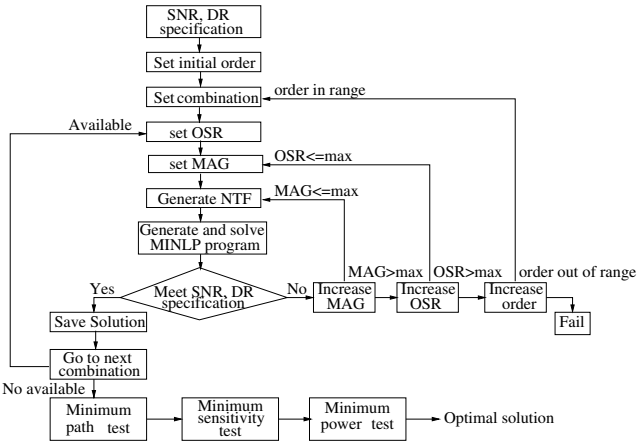

Figure 3: Topology synthesis methodology

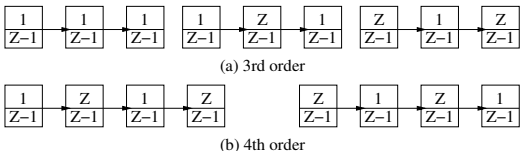

Figure 4: Combinations of integrator types

stability is the global optima. If a test can not differentiate between solutions, other tests, like power consumption, are used.

5. Experiments

We presented experiments for topology synthesis of 3^{rd} and 4^{th} order $\Delta\Sigma$ modulators, and compared our results against traditional topologies.

5.1. 3rd order $\Delta\Sigma$ modulator

The specification was $DR \geq 70db$, or equivalently 11 bits of resolution. Hence, the estimated least order $\Delta\Sigma$ modulator was 3. The initial combination for integrator types corresponded to the first combination in Figure 4(a). The minimum OSR was set to 32 and minimum MAG was set to 1.5. Based on these information, NTF was calculated next. Using the $\Delta\Sigma$ toolbox [14], the synthesized NTF was
$NTF1 = \frac{(z-1)(z^2-1.994z+1)}{(z-0.6685)(z^2-1.529z+0.6629)}$.

With this NTF, the design flow was able to generate an optimal solution with DR of 75db and peak SNR of 67db, which met the specification. For the cost function minimizing the total sensitivity, the optimal topology solutions obtained for the first two combinations of integrator types in Figure 4(a) are shown in Figure 5(a) and (b) respectively. For both topologies the minimized sensitivity is very close to 0. In order to more accurately determine the global optima, Monte-Carlo analysis was carried out for the two topologies. The analysis considered a maximum 10% variation from the nominal value for each of the coefficient variables, and a uniform distribution in the -5% to +5% range for the variation. From the analysis, the second topology turned out to be the least sensitive one.

We compared our solutions with traditional topologies from [14]. In [14], there is no optimization scheme to

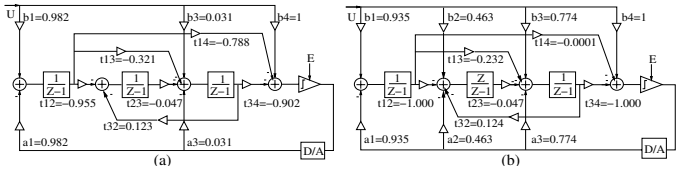

Figure 5: Two synthesized topologies using minimum total sensitivity cost function

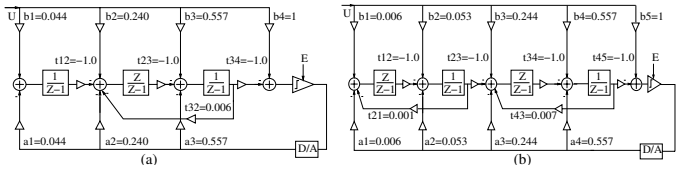

Figure 6: 3^{rd} and 4^{th} order topology from the toolbox in [14]

generate and select an optimal topology. Instead, 4 sets of incomplete topologies with combination of integrator types and signal paths pre-set are stored in a library, and one of these is chosen to derive the complete topology. Figure 6(a) shows one of the complete topologies. To compare its sensitivity, we run Monte-Carlo analysis on the modulator topology. The analysis setting was the same as for the previous experiment. The resulting DR and SNR were compared with those for the topology in Figure 5(b). The first case considered the feasibility of DR and SNR, that is whether the resulting topology can still function as a modulator with an working DR and SNR. The other case considered the deviation of DR and SNR of the resulting topology from the nominal values. In terms of feasibility, a test scheme based on linear regression lines was used, similar to [2]. The results show that 646 out of the total of 1,000 Monte-Carlo runs are still feasible for the topology, as shown in Figure 6(a). 961 out of the 1,000 runs are feasible for the topology with minimum total sensitivity shown in Figure 5(b) (which was generated using the proposed method). In terms of deviation, we consider the DR deviation from the nominal value (75db) for all feasible solutions. The histograms of DR deviation for both topologies are shown in Figure 7. It can be seen that the DR deviation is significant for the topology in Figure 6(a) - produced using the tool in [14], and many feasible solutions have DR deviations higher than $|3db|$. On the other hand, the optimal topology in Figure 5(b) has most of its solutions concentrated in the region of DR deviation less than $|2db|$. So, the synthesized topologies are more tolerant to design parameter variations not only in terms of yield (number of feasible solutions) but also performance deviations.

For the cost function minimizing power consumption, the optimal synthesized topology is shown in Figure 8(a). Note that it used the 2^{nd} combination in Figure 4(a). This topology achieves a total capacitance equal to about 18 units of C_s. Compared to the topology from [14] shown in Figure 6(a), which has a total capacitance of 32 units of C_s, it saved power by 44%.

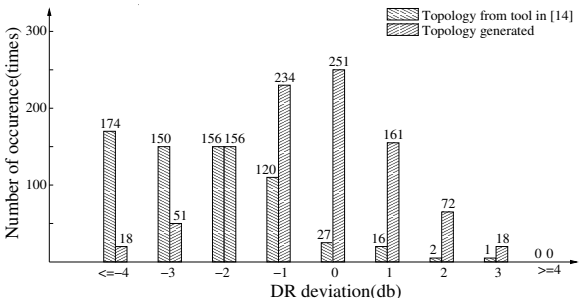

Figure 7: Histograms of DR deviation

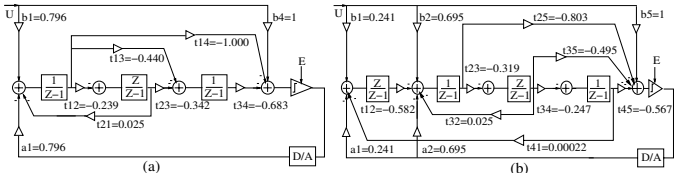

Figure 8: Synthesized topologies using minimum power consumption cost function

5.2. 4th order $\Delta\Sigma$ modulator

The design specification was $DR \geq 80db$ or equivalently 13 bits of resolution. The estimated order for this DR is 4. In this experiment, the initial OSR was set to 16 ($16 \leq OSR \leq 256$) and MAG was fixed to 1.5. The design flow started with the first combination of integrator types shown in Figure 4(b).

We first used the cost function for minimum signal paths complexity. The optimal topology generated in the first iteration does not meet the DR specification. Since MAG was fixed, OSR was increased to 32. Next, using the toolbox [14] the design flow generates following NTF2:

$NTF2 = \frac{(z^2-1.999z+1)(z^2-1.993z+1)}{(z^2-1.492z+0.563)(z^2-1.7z+0.7861)}$

This time, the generated topology had a DR of 84db. Since the specification was met, the design flow went to the other combination of integrator types to generate an optimal topology for that combination. The two optimal topologies generated for the two combinations in Figure 4(b) are depicted in Figure 9 (coefficient values are not shown). There are 12 and 13 signal paths for the topologies in Figure 9, respectively. So, the topology in Figure 9(a) was the global optima with respect to the minimum path cost function. For minimum total sensitivity, the two optimal topologies synthesized for the two combinations of integrator types are presented in Figure 10. Both topologies have their cost value very close to zero. Monte-Carlo analysis shows that the first one is the global optima. We compared these topologies with those from [14]. The toolbox generated the complete topology in Figure 6(b). This topology has 15 signal paths, which is more than the topologies in Figure 9. To compare their sensitivity, we run Monte-Carlo analysis on this modulator topology and the one in Figure 10(a). For the topology in Figure 6(b) - from [14], and the one shown in Figure 10(a), there are 449 feasible solutions out of 1,000 and 905 feasible solutions

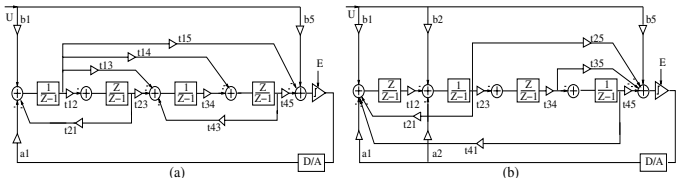

Figure 9: Two synthesized topologies using minimum signal path cost function

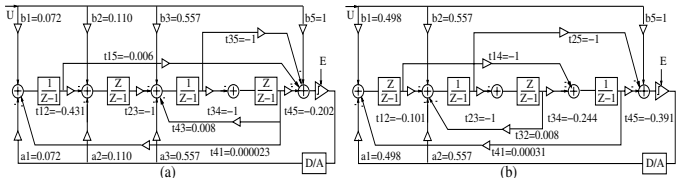

Figure 10: Two synthesized topologies using minimum total sensitivity cost function

out of 1,000, respectively. The later topology achieves a two times better yield as the first one with a maximum 10 % variation of the coefficient variables. Figure 11 compares the DR deviation for the two topologies from the nominal value (84db). For the topology from [14], feasible solutions are scattered in various regions, and there are many solutions that have DR deviation more than $|3db|$. For the optimal topology generated using the proposed methodology, feasible solutions are highly concentrated in the region where DR deviation is less that $|3db|$, and only a small number solutions go beyond that region.

Finally, using the cost function for minimizing power consumption, the optimal topology generated with our method is shown in Figure 8(b). This topology achieves a total capacitance of about 26 units of C_s. Compared to the topology from [14] and shown in Figure 6(b), which has a total capacitance of 38 units of C_s, it saves power by 32%.

To show that the synthesized topologies are effective in terms of DR, the DRs for three topologies (the traditional topology in Figure 6(b), the one in Figure 8(b) optimized for power consumption, and the one in Figure 10(a) optimized for total sensitivity) are plotted in Figure 12. It can be seen that they have similar DR performance.

6. Conclusion

This paper presented a methodology for automated synthesis of single-loop single-bit $\Delta\Sigma$ modulator topologies. To consider all possible topologies, a generic $\Delta\Sigma$ modulator topology was defined, and symbolic TF for this topology were derived. We then formulated the synthesis problem as MINLP. This guarantees finding an optimal solution with respect to the requirements. Experiments showed that the optimal topologies generated by the proposed method are less complex in terms of the number of signal paths, much more resistant to coefficient variations in terms of the yield and performance deviation, and more power efficient when compared to traditional modulator topologies. Ongoing

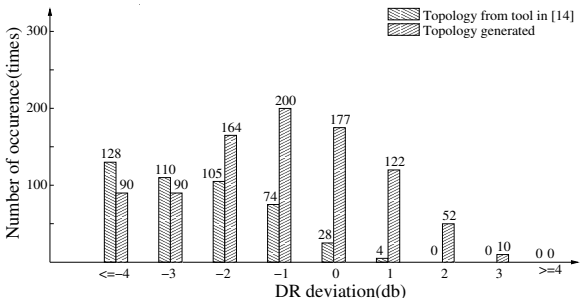

Figure 11: Histograms of DR deviation

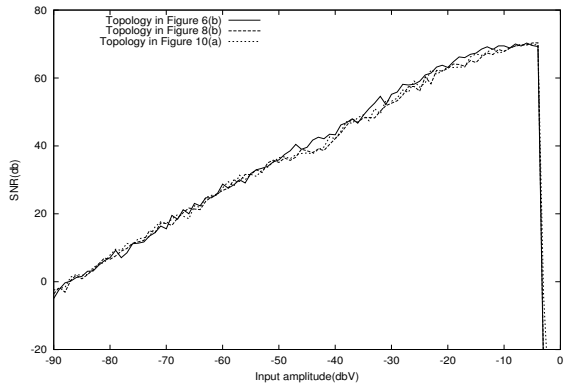

Figure 12: DR Comparison of the topologies

work attempts to extend the methodology to multi-loop and multi-bit $\Delta\Sigma$ modulators.

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