An Introduction to VLSI (Very Large Scale Integrated) Circuit Design

Presented at EE1001
Oct. 16th, 2012

By Hua Tang
The First Computer

The Babbage Difference Engine (1832)
25,000 parts
cost: £17,470
The first electronic computer (1946)
First Transistor (Bipolar)

First transistor
Bell Labs, 1948
The First Integrated Circuits

Bipolar logic 1960’s

ECL 3-input Gate
Motorola 1966
Basic IC circuit component: MOS transistor

MOS: Metal Oxide Semiconductor
**Intel 4004 Micro-Processor**

- 1971
- 1000 transistors
- < 1MHz operation
- 10μm technology
Intel Pentium (IV) microprocessor

2001
42 Million transistors
1.5 GHz operation
0.18μm technology
More recent Processors

2006
291 Million transistors
3 GHz operation
65nm technology

2007
800 Million transistors
2 GHz operation
45nm technology (the biggest change in CMOS transistor technologies in 40 years)

2010 Core i7
1.2 Billion transistors
3.3 GHz operation
32nm technology
Moore’s Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.

- He made a prediction that semiconductor technology will double its effectiveness every 18 months.
Moore’s law in Microprocessors

Transistors on Lead Microprocessors double every 2 years

2X growth in 1.96 years!

Year


Transistors (MT)

1000

100

10

1

0.1

0.01

0.001

1970

1980

1990

2000

2010

4004

8008

8080

8086

8085

486

386

286

Pentium® proc

P6

© Digital Integrated Circuits 2nd

 Courtesy, Intel

Introduction
Lead Microprocessors frequency doubles every 2 years
Not Only Microprocessors

Cell Phone
HDTV
PDA

...
What is a MOS Transistor?

A Switch! \[ V_{GS} \geq V_T \]  

An MOS Transistor \[ |V_{GS}| \]
MOS Transistors - Types and Symbols

- **NMOS**: if $G=\text{“0”}$ or ground, switch on
- **PMOS**: if $G=\text{“1”}$ or $V_{dd}$, switch on
The CMOS Inverter: A First Glance

The CMOS inverter is a fundamental building block in digital electronics. It consists of a p-MOSFET and an n-MOSFET connected in series, forming a voltage buffer. The inverter circuit is characterized by its input voltage $V_{in}$ and output voltage $V_{out}$. The operation of the inverter is based on the voltage levels $V_{DD}$ and the load capacitance $C_L$. The inverter circuit is designed to switch between two stable states, corresponding to the high and low logic levels of a digital system.
CMOS Inverter
First-Order DC Analysis

\[ V_{in} = V_{DD} \quad \rightarrow \quad V_{out} = 0 \]

\[ V_{in} = 0 \quad \rightarrow \quad V_{out} = V_{DD} \]
The delay 
Essentially 
determines the 
clock speed of the 
processor
Static CMOS (Complementary MOS)

PUN and PDN are dual logic networks.

PUN

\[ \text{PUN and PDN are dual logic networks} \]

PDN

\[ \begin{align*}
V_{DD} \\
\text{PMOS only} \\
F(\text{In1, In2, ... InN}) \\
\text{NMOS only}
\end{align*} \]
NMOS Transistors in Series/Parallel Connection

Transistors can be thought as a switch controlled by its gate signal.

NMOS switch closes when switch control input is high.

\[
\begin{align*}
&\text{Y = X if A and B} \\
&\text{Y = X if A OR B}
\end{align*}
\]

NMOS Transistors pass a “strong” 0 but a “weak” 1.
PMOS Transistors in Series/Parallel Connection

PMOS switch closes when switch control input is low

PMOS Transistors pass a “strong” 1 but a “weak” 0
Example Gate: NAND

Truth Table of a 2 input NAND gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
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PDN: $G = AB \implies$ Conduction to GND

PUN: $F = \overline{A + B} = \overline{AB} \implies$ Conduction to $V_{DD}$

$$G(In_1, In_2, In_3, \ldots) = F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \ldots)$$
Example Gate: NOR

Truth Table of a 2 input NOR gate

<table>
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<th>Out</th>
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\[ \text{OUT} = \overline{A + B} \]
**Full-Adder**

![Full-adder diagram](image)

<p>| | | | | |</p>
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<tr>
<th></th>
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<tbody>
<tr>
<td>$A$</td>
<td>$B$</td>
<td>$C_i$</td>
<td>$S$</td>
<td>$C_o$</td>
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<tr>
<td>0</td>
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The Binary Adder

\[ S = A \oplus B \oplus C_i \]
\[ = A\overline{B}\overline{C}_i + A\overline{B}\overline{C}_i + \overline{A}\overline{B}C_i + AB\overline{C}_i \]
\[ C_o = AB + BC_i + AC_i \]
Complimentary Static CMOS Full Adder

28 Transistors
The Ripple-Carry Adder

\[ A_0 \quad B_0 \quad A_1 \quad B_1 \quad A_2 \quad B_2 \quad A_3 \quad B_3 \]

\[ C_{i,0} \quad C_{o,0} = C_{i,1} \quad C_{o,1} \quad C_{o,2} \quad C_{o,3} \]

\[ S_0 \quad S_1 \quad S_2 \quad S_3 \]
SRAM Memory cell
# The add-up

<table>
<thead>
<tr>
<th>Component</th>
<th>Count</th>
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<tbody>
<tr>
<td>32-bit adder:</td>
<td>&gt;3,000</td>
</tr>
<tr>
<td>32-bit comparator:</td>
<td>&gt;3,000</td>
</tr>
<tr>
<td>32-bit multiplier:</td>
<td>&gt;50,000</td>
</tr>
<tr>
<td>1k SRAM:</td>
<td>6,000</td>
</tr>
<tr>
<td>...</td>
<td></td>
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</table>
Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function
Future Design Challenges

- Processor architecture (multiple-core; interconnections)
- Semi-conductor materials (current leakage; process variation)
- Power consumption (power density; thermal dissipation)
Career in VLSI design

VLSI circuit design and design automation

- Intel, IBM, AMD, Texas Ins., Agilent,…
- Qualcomm, Broadcom, Samsung,…
- Micron, Seagate, WesternDigital…
- Cadence, Synopsys, MentorGraphics…
- Xilinx, Altera, ….
VLSI Design: FFT Butterfly

- Widely used in signal processing
- Design Butterfly Unit for 2-point FFT
- Components include multiplier, adder, subtractor, and data management

By: Spencer Strunic
Matt Webb
FFT Butterfly Unit Layout
VLSI Design: 8-bit CPU

- **Registers**
  - Store data
  - Manipulate data

- **ALU**
  - Select between many different operations to output

- **Adder**
  - Adds two 8-bit numbers

- **Multiplier**
  - Multiplies two 8-bit numbers

By: Brian Linder
Matt Leines
8-bit CPU Layout
FIR Filter

- FIR – Finite-Impulse Response
- Involves calculations of finite convolution sums in discrete-time systems
- Useful for Digital Signal Processing
- Equation -

\[ y[n] = \sum_{k=0}^{N-1} h[k]x[n - k] \]

- \( x \) is the input signal, \( h \) is the finite impulse response, \( y \) is the sum output and \( N \) is the order of the filter
FIR Filter System Design

Module 1 – Control Module
Module 2 – Input Module
Module 3 – Coefficients Module
Module 4 – Arithmetic Module
Module 5 – Results Storage
A Delta-Sigma Converter for WCDMA

By: Matt Webb, Hairong Chang
Nowadays, many electronic systems on a single chip have both analog and digital (called Mixed-signal SoC (System on Chip))

From Texas Instruments
Why A-D Interface?

- Nature is analog, not digital.
- A-D interface’s role is “translator”.

Analog World
- Twisted Pair Wires, Phone Lines
- MEMs Sensors, Actuators
- RF Electro-Magnetic Waves
- Microphones, Audio Devices

Digital World
- Storage Media
- Imagers, Display

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Introduction
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