EE 2212 **FINAL EXAM** **Name:_____**

(On-Line Format) **S. G. Burns**

15 December 2021

Note 1: Verify that you have good Internet connectivity for the Final Exam!!!

Note 2: I will post the Final Exam at 10 am, Wednesday 15 December, on the EE 2212 WEB Page and CANVAS

Note 3: I will remove the posting at 11:50.

Note 4: Use either a printed download from the EE 2212 WEB page, CANVAS or separate sheets of paper or a combination. Be sure your name is on each sheet of the submitted material. Be sure your solutions are legible; do recognize the capabilities of your scanner and imaging systems as well as room lighting.

Note 5: Your audio and video must be turned on during the exam. This is to facilitate responding to any questions you might have.

Note 5: Submit a pdf and/or WORD and/or jpgs of your solutions as attachments to an e-mail to me sburns@d.umn.edu by noon.

Note 6: Open Book, Laptop, WEB access OK, Tablet, etc. and Notes. All of these sources are what you might be expected to exploit as an engineer in an industrial environment. Watch your time management if you surf the WEB!

PROBLEM	TOPIC	POINTS	SCORE
1	**Operational Amplifiers**	30	
2	**Semiconductor , MOSFET and Photonics Pot-Pourri**	66	
3	**CA 3130 BiMOS Operational Amplifier Analysis**	56	
4	**µA 741 Circuit Analysis-Power Amplifier**	48	
TOTAL		200	

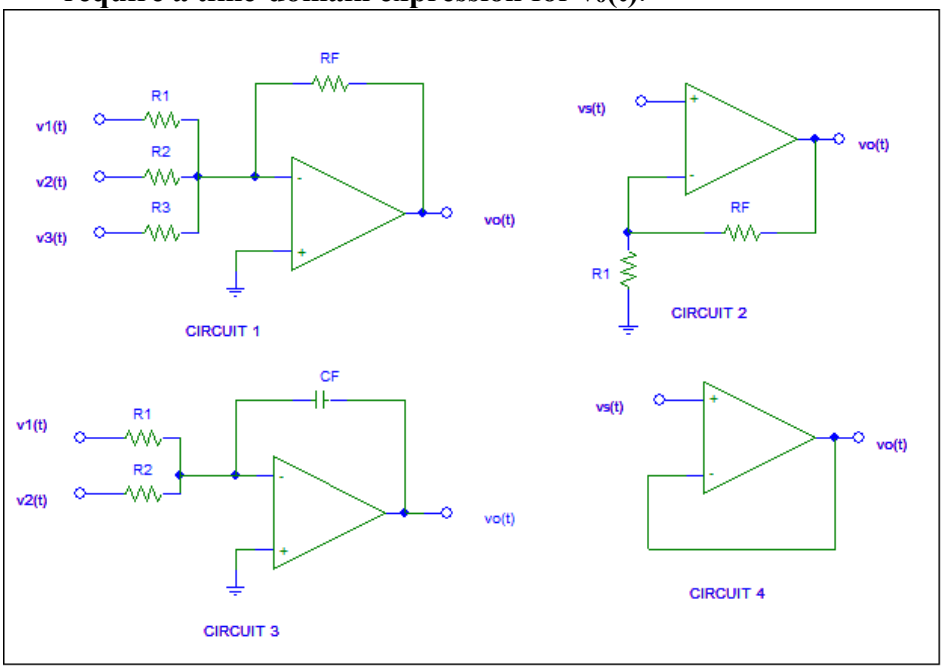
Problem 1 (30 Points) Operational Amplifier Specifications and Circuits

(a) (10 Points) Should be no surprise here. Provide numerical values for the operational amplifier specifications:

Specification	Ideal Operational Amplifier	µA 741 Typical Values	CA 3130 BiMOS Typical Values
Voltage gain			
Input Resistance			
Output Resistance			XXXXXXXXXX
Unity Gain Bandwidth			XXXXXXXXXX

(b) (20 Points; 5 Points for each circuit) Operational Amplifier Basic Circuit Topologies

Assume ideal operational amplifiers therefore you can use summing point constraints. Write an expression for $\mathbf{v_o(t)}$ for each of the four circuits. Observe that no numerical calculations are required. Note-**time domain input voltages require a time-domain expression for $v_o(t)$.**



Circuit 1 $v_o(t)$ =

Circuit 2 $v_o(t)$ =

Circuit 3 $v_o(t)$ =

Circuit 4 $v_o(t)$ =

Problem 2 (66 Points; 11 Points Each) Semiconductor , MOSFET and Photonics Pot-Pourri

(a) For Si, list two donor elements and two **non-metallic** acceptor elements:

TWO DONOR ELEMENTS	TWO ACCEPTOR ELEMENTS
1.	1.
2.	2.

(b) Assume two samples of doped Si; the doping concentrations N_D and N_A are the same for each sample and each sample is at the same temperature. The mobility, μ, of the n-doped sample is **(HIGHER, LOWER, ABOUT THE SAME**) compared to the p-doped sample and . the resistivity, ρ, of the n-doped sample is (**HIGHER, LOWER, ABOUT THE SAME**) compared to the p-doped sample.

(c) At T = 0K, the intrinsic carrier density in Si is (**∞, 0, 1.0 x 10^{10}, 5 x 10^{22}**) cm^{-3} and at T = 300K the intrinsic electron concentration of Si is (**∞, 0, 1.0 x 10^{10}, 5 x 10^{22}**) cm^{-3} and the intrinsic hole concentration is (**LARGER ABOUT THE SAME, SMALLER**) than the intrinsic electron concentration and this compares to the atomic density of crystalline Si which has about (**1.5 x 10^{10}, 10^{18}, 5 x 10^{22}, Undetermined**) atoms/cm^3.

(d) As the gate oxide thickness decreases in a MOSFET, the threshold voltage, V_T, (**INCREASES, DECREASES, ESSENTIALLY REMAINS THE SAME, IS 26 mV AT 300°C**) and as the channel doping density between the source and drain increases in a MOSFET, the threshold voltage, V_T, (**INCREASES, DECREASES, ESSENTIALLY REMAINS THE SAME, IS 26 mV at 300°C**).

(e) Compute the emission wavelength, λ, associated with GaN, which is a key material for LED lighting, and the λ you computed is in the (**Infrared, Red, Yellow Green, Blue, Near UV**) portion of the spectrum, however To achieve "white" light a (**Magenta, Green, Yellow, Cyan, Red**) phosphor coating is used

(f) In considering the design of a solar photovoltaic panel, engineers typically use a solar insolation constant value of (**200 watts/m^2, 1 kW/ft^2, 1 kW/m^2, 1 kW/cm^2**) and for each of the 1.5 m^2 solar panels on the top of Malosky stadium, you can expect about 200 watts peak power output on a sunny day (which does happen in Duluth). Consequently, the efficiency of this solar panel is about (**5%, 10%, 13%, 20%, 40%, 100%**) but it should be noted that design and manufacturing improvements since these were installed now yield efficiencies of about (**5%, 10%, 13%, 20%, 40%, 100%**).

Problem 3 (56 Points 7 Points Each) CA 3130 BiMOS Operational Amplifier Analysis

We discussed the design and analysis of this BiMOS amplifier in class. This problem is designed to review key elements of these discussions. The next page includes an annotated circuit diagram of an Intersil CA 3130/CA 3130A BiMOS Operational Amplifier. Assume:

- V^+ = +12 volts and V^- = -12 volts.
- Neglect any current in R_1.
- All BJTs have a β = 100.
- V_J = 0.7 volts

Answer the following questions. Each question is equally valued at 5 points.

(a) What is the function of D_5, D_6, D_7, and D_8? Short answer.

(b) Why is the input differential resistance, R_{id}, between Pins 3 and Pin 2 significantly much higher (orders of magnitude) than might be found if a BJT input differential amplifier was used for the first stage? Answer in terms of the MOSFET construction and fabrication. Short answer.

(c) Provide numerical a numerical value for the Q_{11} transconductance, g_m . Note that I_{C11} = 200 μA.

(d) Provide numerical a numerical value for input resistance, r_π, of Q_{11}? Hint: Use Part (c) results and recall the assumption that $\beta = 100$.

(e) Estimate a value for the dc voltage at the R_1 - Z_1 node? Recall, you are to neglect the current in R_1.

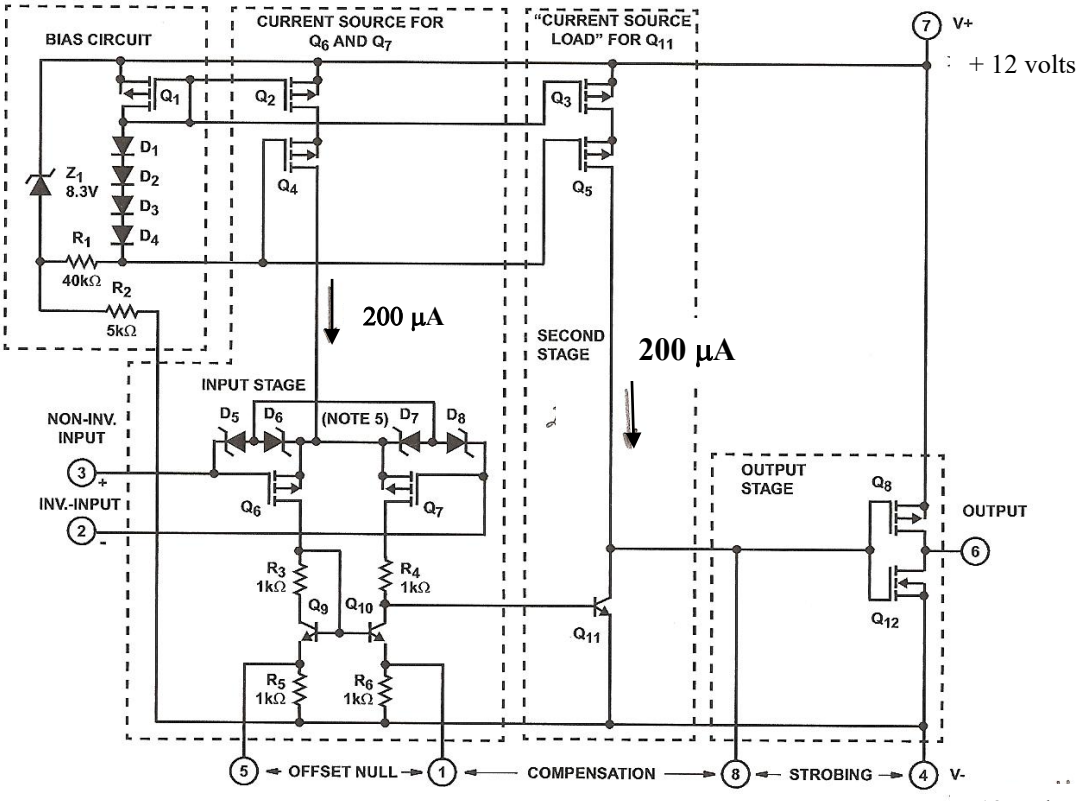
(f) Using your value from Part (e), estimate a value for the current in R_2?

(g) Using your value from Part (e), estimate the dc voltage at the connected gate nodes of Q_1, Q_2, and Q_3. Hint: Recall from the assumptions listed above that for a diode, $V_J = 0.7$ volts.

(h) Estimate a value for (Hint: Good idea to assume high β and circuit symmetry):
I_{C6}_____ I_{C7}_____ I_{C9}_____ I_{C10}_____

CA3130, CA3130A

Schematic Diagram



NOTE:

Problem 4 (48 Points; 8 Points Each) µA 741 Circuit Analysis-Power Amplifier
Assume V+ =12 volts and V- = -12 volts. $V_{BE(on)}$= 0.7 volts. R_L = 2 kΩ connected to the OUTPUT terminal. Answer the following questions:

(a) The configration of Q_{11}, Q_{10}, Q_{12}, and Q_{13} is a (**Class A, Class B, Class C, ClassAB**) amplifier

(b) If $v_o(t) = 10\cos(\omega t)$ volts, compute the peak and average power in R_L = 2kΩ.

(c) If $v_o(t) = 10\cos(\omega t)$ volts, compute the collector efficiency, η_C = _____ % and if $v_o(t) = 12\cos(\omega t)$ volts, compute the collector efficiency, η_C =_____%

(d) If $v_o(t)$ is a 24 volt, peak -to-peak square wave, the power dissipation in Q_{14} and Q_{20} approaches (**72 mW, 36 mW, 0 mW, π/4x(12/24) mW**) Circle your choice.

(e) The voltage gain of the Q_{14}-Q_{20} circuit is about (**200,000, -1.0, +1.0, Computed from $-g_mR_L$**) Circle choice.

(f) The Q_{15} circuit operates to limit the Q_{14} collector current to what value?