ECE 1315 - Lab #10: Data Selector

Important note: If the DE1 boards are operational, you will download your design and test it on the board using the DIP (Digital InPut) switches and Light Emitting Diodes (LEDs). As a result, when you create your project, make sure to select the **Cyclone II 2C20** as the FPGA.

Goal: Design a circuit that generates the function $f(X_3,X_2,X_1,X_0)$ using an 8→1 data selector, the 74LS151, in four different ways simultaneously in QuartusII.

$$f(X_3,X_2,X_1,X_0) = \Sigma m(0,2,4,5,6,7,10,12,14,15)$$

Use a different combination of three variables on the select inputs of the data selector in each version of your circuit so that the data inputs on your data selectors are functions of different variables in each version. Your circuit will include four MUXes (one for each version of the function implementation) plus possibly a NOT gate to complement some of the variables. In other words, in the four versions of your circuit use the following variables:

Select inputs	Data inputs functions of...
X_3, X_2, X_1	X_0
X_3, X_2, X_0	X_1
X_3, X_1, X_0	X_2
X_2, X_1, X_0	X_3

The MUXes can be found under the name "81mux" (an 8 input, 1 output mux) or 74151 (the part name). **Note: A, B, C are equivalent to S_0, S_1, S_2, respectively (the order matters!).**

Display the outputs of the four data selectors on F_3, F_2, F_1, and F_0 in QuartusII. Furthermore, assign the input pins to the four (4) right-most DIP switches and the outputs to the four (4) right-most LEDs. Obviously, these four outputs should all display the same function. Be sure that you know which of the select inputs on the MUX is the most significant in numbering the data inputs. Do not forget to connect the MUX's enable (sometimes called "strobe") to its active level, 0. Also note that the MUX provides both the normal data selector output and its complement.

Test your circuit as you did with combinational circuits in earlier labs, using the vector waveform in QuartusII to generate the inputs to your circuit and to capture the outputs of your circuit. It might be useful to assign the inputs and/or the outputs as busses using []'s after the name of each pin (e.g. x[3], x[2], x[1], x[0]). Also, demonstrate the functionality of your design via the DIP switches and LEDs on the DE1 board. Minimize the total number of "gates" you use in your four versions of the function implementation beyond the necessary 4 MUXes.

Be sure to have your lab instructor sign his/her sheet once you have demonstrated your working circuit to him/her and have answered the questions below. In your lab report, include screenshots of your bdf and the output of your vwf file.

Q#1: Why is a MUX (multiplexer) also called a "selector"?
Q#2: Why are MUXes useful when designing combinational logic? (for one possible answer, think how they're similar to iterative design in general)