

ECE 1315 - Lab #5: Latches and Flip Flops

Latches are useful devices that contain feedback and thus enable memory. They are used in applications such as simple noise filtering circuits and flip-flops. The first latch discussed in class was the SR/S'R' Latch which allowed us to Set or Reset the output. The drawback of such a latch was that it contained a transition that caused a metastable (indeterminate) state. A clock/enable signal was then added to prevent such a transition when the clock signal was low. Lastly, the Gated D-Latch eliminated this altogether by preventing S and R from changing at the same time. Hence, in our discussion the latches have become progressively more stable.

A convenient way to implement a Gated D-latch is shown below in Figure 1 (C = Clock/Enable).

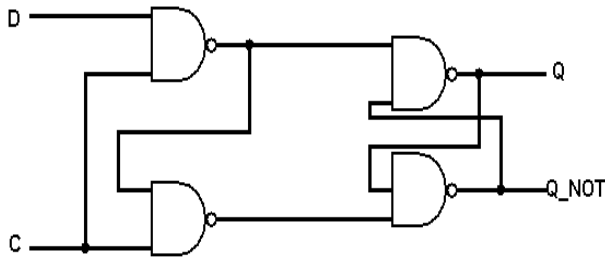


Figure 1: Gated D-Latch

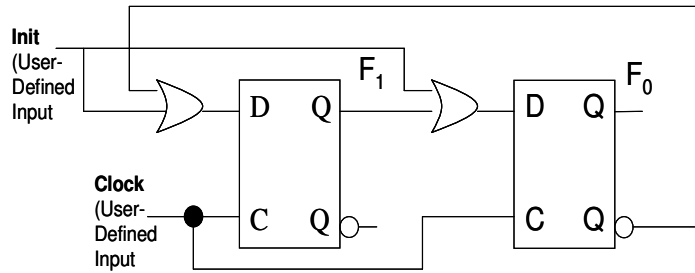


Figure 2: Two Master-Slave D Flip Flops

(1) Build the Gated D-Latch in Quartus II using four (4) NAND gates, two input pins (for D and C), and two output pins (for Q and Q_Not). The Quartus II Supplement PDF (<https://www.d.umn.edu/~pjweber/ece1315f07/umdonly/labs/QuartusIISupplement.pdf>) on the References page of the course website will be useful for doing this. Test the circuit by creating a Vector Waveform with all possible combinations for D and C, where D and C do *not* change at the same time. Save a screenshot of the waveform for your report and try to determine the state table for the latch. *Leave the Block Diagram File (bdf) open as you will continue to use it.*

One Master-Slave D Flip-Flop (**not shown**) is built from *two* of these Gated D-latches. The master latch (first one) is exactly as shown above, but the slave latch (second one) uses a complemented control signal, so that the master latch captures information when the control signal is logic 1 and then transfers that information to the slave when the control signal is logic 0.

(2) Build one Master-Slave D Flip-Flop in Quartus II by first creating a symbol file of your Gated D-Latch. In a new bdf file, insert this new symbol twice along with a NOT gate and configure the Master-Slave D Flip-Flop as described in the above paragraph (you will again need two input pins and two output pins, which should have *different* names than in the Gated-D Latch bdf). Test the circuit by creating a Vector Waveform with all possible combinations for D and C (again, they should *not* change at the same time). Save a screenshot of the waveform for your report and try to determine the state table for the flip-flop. *Leave the .bdf open as you will continue to use it.*

(3) Build *two* Master-Slave D flip-flops (*four* Gated D-latches) connected as shown in Fig. 2 by creating a symbol for your Master-Slave D Flip-Flop (as you did previously for the latch) and placing them appropriately in a new .bdf file. Test the circuit by creating a Vector Waveform, keeping "Init" high until after the first falling edge of your clock signal and then leaving it low for the remainder of the simulation, and determine the repeating pattern. Save a screenshot of the waveform for your report.

For your report, show each of the three Vector Waveform screenshots and explain the differences and similarities between latches and a flip-flops. **Also specify what repeating pattern you observed.** Have your lab instructor check your result and sign his/her sheet once you've answered the question(s).

Q#1: How do latches and flip flops differ? How are they similar?

Q#2: What type of timing and init. problems can arise with the Vector Waveform files of Quartus II?