ECE 1315 - Lab #7: Finite State Machine

Design a (modular) 6-state synchronous finite state machine in Quartus II, implementing a counter that steps through the following sequence on the output variables $z_2z_1z_0$ as the clock ticks:

z_2 z_1 z_0	Decimal Notation*
0 1 1	3
0 1 0	2
1 1 0	6
1 0 1	5
1 1 1	7
0 0 0	0

* - Possibly useful in Quartus II

This 6-state pattern repeats forever. There are no input variables to this state machine. Be sure that the circuit is entirely synchronous, i.e. the system clock signal (from a user-defined input pin in Quartus II) goes to the clock input on all flip-flops you are using and nowhere else.

Verify the functionality of your design with a Vector Waveform File and record the sequence of states that the circuit ends up repeating. Also, take a screenshot of the waveform to include in your report. Note that the initial state of the circuit is unpredictable, so you cannot control that. Do not be concerned about whether or not your circuit is self-starting. It is possible (though unlikely) that your circuit will *not* be self-starting and might get stuck in one or more of the unused states. If that happens, your lab instructor will show you how to get out of that undesired pattern. For debugging purposes, you might find it helpful to display also your state variables (flip-flop Q outputs) if they are different from your output variables.

Clearly your design will need at least three flip-flops, because it uses six states (you can use more if it helps minimize the total number of chips/gates). For your functions, use any of the parts in Quartus II that correspond to those found in Table 1. To maximize your score in this lab, minimize the total cost of your implementation given the component costs shown in Table 1.

Table 1: Available Logic Elements and Associated Cost

Logic Element(s)	Associated Cost
NOT Gate	2
2-input NAND, NOR, XOR, XNOR	4
2-input AND, OR 3-input NAND, NOR	6
3-input AND, OR	8
JK Flip Flop	12

For your report, show the state diagram you generated for your counter, the steps you took to generate your design (tables and Karnaugh maps), and the pattern you observed to record the operation of your circuit. Remember to get your lab instructor to check your result, and sign his/her sheet with the cost of your implementation after you've answered the question(s).

Q#1: How many unused states were there in your design were there?
Q#2: How did you use these unused states? What possible drawback might there be to this approach?