

QuartusII Debugging Questions

-Have you authenticated at <http://port.d.umn.edu>?

(QuartusII will not be able to access the web license and might freeze)

-Do you have a project open?

(Compilation, Simulation, etc. will not be options)

-Are all of your project files in your project folder?

(The project might not be able to find them)

-Did you use legal names for your pins, etc.?

(Names cannot be repeated nor contain special characters like '>', '=', etc. and spaces)

-Did you set the top level entity to the file you are trying to compile?

(QuartusII compiles the top level entity specified under Assignments→Settings→General→Top Level Entity)

-Did you specify the waveform file you are trying to simulate?

(QuartusII will simulate the waveform file of the same name as your project unless you specify a different one under Assignments→Settings→Simulation→Simulation File)

-Did you allow adequate time for propagation delays in your simulations, i.e. configure changes far enough apart?

(QuartusII simulates timing delays so events do not take place instantaneously)

-Are individual pins of a bus group labeled name[#], with the MSB as name[largest #] and the LSB as name[0]?

When using Verilog:

-Did you save the file as *.v?

-Did you name the module?

-Is "endmodule" all one word?

-Are all your inputs/outputs defined?

-Are busses labeled [n-1:0]name, where n indicates the width of the bus?

-Are pins/busses that are set to values within an always@() section labeled as reg(isters)?

-Does code to be executed after an "if" statement start with "begin" and end with "end"?