

## ECE 1315 – Quartus II Supplement

The following is designed to be a *very brief* introduction to the Quartus II tool suite from Altera. For a more complete guide, please follow the tutorials provided with the software.

**Important:** Before starting the Quartus II software, you **must** authenticate the computer so that it can access the necessary web license from Altera’s website—most of the useful functionality of the software will not be enabled otherwise. To do this, log on at <http://port.d.umn.edu/> using your user id and X.500 password. Also, it is a good practice to log off the computer when you are done by returning to the same web page and clicking the “logout” button.


-Generally, you will need to start a new project by clicking on File → New Project Wizard. When prompted you can click “Next” or “Finish” with the exception of the notes below:

- You must save your design in the “only place to save” on the desktop.
- You may select any device to map the pins to if you are only using the software (i.e. not downloading your designs onto Altera hardware).
- No Tools need to be selected.

-When creating a Block (logic) Diagram File (bdf) (click on File → New), you can insert parts by clicking on Edit → Insert Symbol or by clicking the AND gate button (Symbol Tool). Within the subsequent pop-up window, the following might be useful (arrows indicate a subfolder):

- Flip Flops: Primitives → Storage → jkff (JK Flip Flop), etc.
- Gates: Primitives → Logic → nand2, and2, or2, not, etc.
- Power & Ground: Primitives → Other → vcc, gnd
- I/O Pins: Primitives → Pins → input, output\*

\*Outputs and inputs that you want to view later must be connected to an output or input pin.

-Tips: You can add wires by clicking and dragging when you select the  tool. Also, within your bdf, x’s are generally indications of extra wires.

-Once you have created a logic diagram, you will need to compile your design to create the appropriate information for the software to simulate the timing of it. Some useful settings to select to speed up the compilation process under Assignment → Settings are Fast Fit (under Fitter Settings) and Use Smart compile (under Compilation Process Settings). You can compile your design by clicking on Processing → Start Compilation. Note: In order to compile a file, you must have an open project. As a result, you need to open the whole project (not just the bdf file) if you save your work and retrieve it later.

-Once you have compiled your design, you can view the timing analysis of it by creating a Vector Waveform File (vwf) (File → New → Other Files). The first step is to select nodes to include in your analysis. You can do so by right clicking in the inputs column on the left and then choose the “Insert Node or Bus...” option. Next, click on “Node Finder...” and then “List”. Make sure the Filter is set to “Pins: all” and then select the nodes you are interested in. Lastly, click the ‘>’ button to add them and then click “OK.” In the vwf, you can set the inputs to different values using the button that is a double-pointed arrow with crossing signals behind it—simply click and drag the mouse over the area that you want to change the waveform value of. Some other useful commands when using vwf’s are:

- Edit → End Time (specifies the length of the timing window)
- View → Fit in Window
- Process → Start Simulation

### More Useful Notes

- When using inputs and outputs that are more than one pin, you can simply enter one pin and then rename it as a series of pins by adding brackets. For example if you wanted a 4-bit input called X, you could rename the pin X[3..0].
- You can create symbols of Verilog code by clicking on File → Create/Update → Create Symbol Files for Current File. You can then access the file by entering a new symbol and looking under your project directory.
- When simulating designs in the Vector Waveform File, always remember to leave adequate time for propagation delays.
- When using busses (multiple pins assigned to a single variable) in the Vector Waveform File, you can change the value type (radix) to be a signed decimal (or other useful types) by double clicking on the Value column and selecting the appropriate choice from the subsequent pull-down menu.
- On the toolbar to the left of the diagram, selecting “Rubberbanding” allows the wires to stay connected when you click and drag them. Also, selecting “Partial Lines” allows the computer to attempt to display a neater format with less crossing of wires/parts.
- When simulating designs in the Vector Waveform File, inputs can be set to count through all possible combinations or individual bits can be set as clocks with successive bits having twice the period of the previous bit if trying to mimic a truth table (binary counting).