EE 1315 DIGITAL LOGIC LAB

EE Dept, UMD

EXPERIMENT # 10: Synchronous Sequence Detector

Design and build a synchronous sequence detector that detects a bit-pattern "1010" using JK-ffs. Please follow the steps provided in the result section.

Use the fjkc symbol in the Xilinx ISE library for this lab. Be sure to properly connect the CLR pin of the symbol to assure proper operation of the flip flop. When connecting the clock input to the flop flops, use the clock component used in previous labs. Again be sure to add the module to your project found at **C:\Xilinx\debounce\debounce.vhd** to allow the program to properly create the programming file. The beginning schematic should appear similar to Figure 1. Your job is to add the logic gates that will be needed for the detection of the bit pattern.

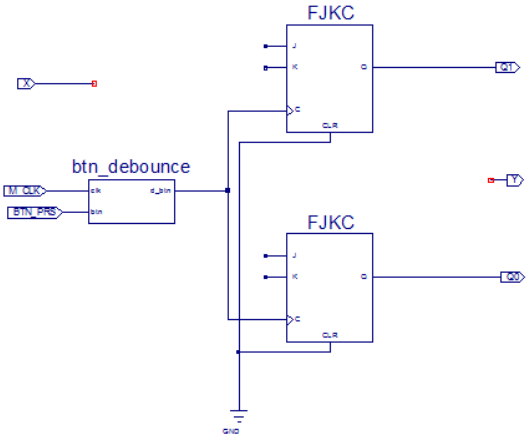

Figure 1: Schematic before adding logic for sequence detection

The input will be supplied to port X from a slide switch. The output will be seen on port Y on a LED. When the slide switch is raised and the clock ticks (button is pressed) a '1' is detected by the circuit. Likewise when the slide switch is down and the clock ticks a '0' is detected. When the specified sequence is detected, Y should show a '1' and the LED will light up. Any other sequence should cause Y to be a '0', leaving the LED unlit. Again, Q1 and Q0 have been added to aid in debugging and to aid in visualization of the state changes in the circuit. Use the following table for your port assignments.

Scalar Port	X	Y	M_CLK	BTN_PRS	Q1	Q0
Site	G18	J14	B8	B18	E17	K14
I/O	SW0	LD0	50MHz	BTN0	LD4	LD3

EXPERIMENT #11 RESULTS

(Print the following pages and bring them with to the lab session)

Your Name: _____

Witnessed by Instructor or TA: _____

Date _____

Show your design process.

Step 1) Derive the State Diagram for "1010" sequence detector

Step 2) Derive the State Excitation Table

Step 3) Derive the FF Input Equations and the Output Equation based on the State Excitation Table

Step 4) Draw the Final Circuit Diagram

Step 5) Build the Circuit (FPGA)

Step 6) Design and generate a desired test Input Pattern that can thoroughly test your circuit

Test Input Sequence Pattern:

X(input)																		
Y(output)																		

Step 7) If the sequence detector works correctly, have your TA approve the result.