EE 1315 DIGITAL LOGIC LAB

EE Dept, UMD

EXPERIMENT # 2: NAND and NOR

Implement each of the following two functions using only four identical logic gates.

$$f_1(w, x, y) = \overline{x} + \overline{w} \cdot \overline{y}$$
$$f_2(w, x, y) = (\overline{w + x})(\overline{x + y})$$

The gates to be used are **NAND** and **NOR**. Therefore, you will need to create **AND** out of **NOR** or **OR** out of **NAND** to implement the given function. This is achieved using a digital logic principle called "DeMorgan's Law."

DeMorgan's law states that "complement (=inversion) of **OR** is **AND** of complements" or "complement of **AND** is **OR** of complements," that is,

$$\overline{(x + y)} = \overline{x} \cdot \overline{y}$$
$$\overline{(x \cdot y)} = \overline{x} + \overline{y}$$

Since DeMorgan's law provides **OR** out of **AND** or vice versa, it allows you to implement **AND** using **NOR** or **OR** using **NAND**. This is one of the unique features of digital logic and the learning objective in this experiment. You should also recognize that a **NAND** or **NOR** gates can be used as inverters. The **NAND** or **NOR** gate is often referred to a universal gate, which means that you can build any logic circuit using **NAND**'s or **NOR**'s only.

Regarding the definition of **AND**, **OR**, **NOR**, and **NAND**, please learn from the Lab #1 results (i.e., the truth table).

After learning the basic principles, design and build the circuits of the given equations, and use the LED's on the Nexys board to verify the logic of your circuit (see Table 1 for the assignment of Scalar Ports). Since both functions have three inputs, you will need to use three switches from the board to represent your inputs. **Record the truth table in the Results section** when you believe that your circuits work properly. Have your instructor or TA verify the results and your schematic and let them sign your results sheet. That is it. See you next week.

Table 1: Scalar Port Assignments

	Inputs			Outputs	
Scalar Port	**w**	**x**	**y**	**f1**	**f2**
Nexys I/O	**SW0**	**SW1**	**SW2**	**LD0**	**LD1**
Site	**G18**	**H18**	**K18**	**J14**	**J15**

The Result Sheet is on the next page.

EXPERIMENT #2 RESULTS

(Print out this page and bring to the lab session)

Your Name: _____

Witnessed by : _____

Date _____

Draw your circuit diagram here:

Truth table of your circuit observed from the F:

w	**x**	**y**	**f_1**	**f_2**
0	0	0		
0				
0				
0				
1				
1				
1				
1				