EE 1315 DIGITAL LOGIC LAB

EE Dept, UMD

EXPERIMENT # 3: Logic minimization in terms of the number of gates

Implement the following function

$$f(w,x,y,z) = w \cdot \bar{x} + \bar{w} \cdot \bar{y} \cdot \bar{z} + \bar{w} \cdot \bar{x} \cdot z + \bar{w} \cdot \bar{x} \cdot y \cdot \bar{z}$$

using only five gates or less. The gates you are allowed to use are two-input AND, OR, NAND, NOR, and NOT gates. An inverter is counted as a single gate. Please algebraically manipulate the given function to derive a minimized equation and the circuit diagram that uses a minimum number of gates. Use the LED's on the Nexys board to verify your circuit and record the truth table. When your circuit works properly, have your instructor or TA sign the Results sheet and verify the number of gates used in your schematic.

The port assignment can be seen in Table 1. Please design and prepare your circuit diagram before the actual lab session.

Table 1: Scalar Port assignments

	Inputs				Output
Scalar Port	**w**	**x**	**y**	**z**	**f**
Nexys I/O	**SW0**	**SW1**	**SW2**	**SW3**	**LD0**
Site	**G18**	**H18**	**K18**	**K17**	**J14**

EXPERIMENT #3 RESULTS

(Print these 2 pages and bring with to the lab session)

Your Name: _____

Witnessed by : _____

Date _____

Number of gates used: _____

Show your minimization process by algebraically manipulating the equations:

Circuit Diagram:

Truth Table Observed From Nexys Board:

w	x	y	z	f
0	0	0	0	
0				
0				
0				
0				
0				
0				
0				
1				
1				
1				
1				
1				
1				
1				
1				