

EE 1315 DIGITAL LOGIC LAB

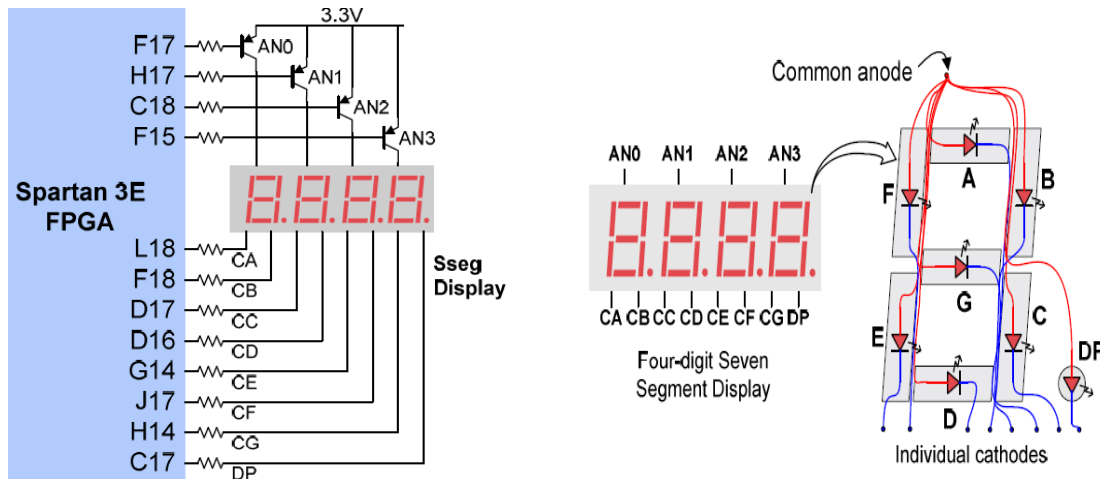
EE Dept, UMD

EXPERIMENT # 5: Combinational logic application design: 7-segment decoder

Combinational logic can be designed by following a standard design procedure as follows:

1. State the problem
2. Determine the required number of input and output variables
3. Assign the input and output variables to letter symbols
4. Derive the truth table
5. Simplify the function
6. Draw the circuit using gates
7. Implement and test the circuit

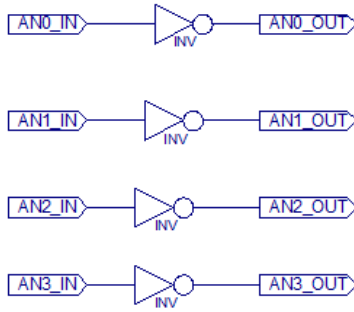
Given problem: Design and implement a 7-segment decoder. This module should take a four bit binary number and output a 7 bit vector that will properly light the 7-segment display patterns on the Nexys-2 board. The configuration of the 7 segment display can be seen below.



In this lab, the right four switches (SW3-SW0) on the Nexys board will be used to represent a four bit binary number, and the left most switched (SW7-SW4) will be used to select which of the 7-segment is activated. Notice that the common anode on each digit of the display is active (3.3V) when logic 0 is present on the Scalar Ports F17, H17, C18, and F15. Also notice each individual cathode will cause the segment in the display to light only when it is logic 0, as this provides a path from the positive voltage to ground through the LED on each segment. Therefore, to display a 0 on the 7-segment display, the cathodes A, B, C, D, E, and F must be logic 0 while cathode G must be logic 1. Simply put, all segments as well as the anode of each digit are negative enabled. The first two entries on the truth table are completed for you in the results section, please complete the table. Since we are not interested in the four digit binary numbers greater than 9, all values 10 and up can be considered don't cares.

After you have completed the table in the results section, find the output functions for each of the individual cathodes in the circuit as a function of the input variables.

The circuit then needs to be created in a schematic and tested. The common anode selectors can be created using NOT gates. By placing four NOT gates with I/O ports on either side as seen below, the anodes can be turned on by raising the switch corresponding to that anode. The scalar port assignments are as follows.



Scalar Port	A0_IN	A1_IN	A2_IN	A3_IN	D3	D2	D1	D0	A0_O	A1_O	A2_O	A3_O
Nexys I/O	SW4	SW5	SW6	SW7	SW3	SW2	SW1	SW0				
Site	L14	L13	N17	R17	K17	K18	H18	G18	F17	H17	C18	F15

Scalar Port	A	B	C	D	E	F	G
Nexys I/O	CA	CB	CC	CD	CD	CD	CG
Site	L18	F18	D17	D16	G14	J17	H14

Table 1: Scalar Port Assignment

Save this project after you have it working. It will be used in a later lab exercise and the reuse of this circuit will save you the effort of redesigning a seven segment decoder.

EXPERIMENT #5 RESULTS

(Print the following pages and bring to lab session)

Your Name: _____

Witnessed by

Instructor or TA: _____

Date _____

Step 1: State the problem

Step 2: Determine the number of required inputs and outputs

No of inputs: _____

No of outputs: _____

Step 3: Assign the input and output variables to letter symbols

Step 4: Construct the truth table of the 7-segment decoder (negative enabled).

Decimal	D3=MSB	D2	D1	D0=LSB	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0							
3	0	0	1	1							
4	0	1	0	0							
5	0	1	0	1							
6	0	1	1	0							
7	0	1	1	1							
8	1	0	0	0							
9	1	0	0	1							
10	1	0	1	0	X	X	X	X	X	X	X
11	1	0	1	1	X	X	X	X	X	X	X
12	1	1	0	0	X	X	X	X	X	X	X
13	1	1	0	1	X	X	X	X	X	X	X
14	1	1	1	0	X	X	X	X	X	X	X
15	1	1	1	1	X	X	X	X	X	X	X

Step 5: Simplify the function. Remember to use XOR gates if necessary. It can reduce gate counts.

Step 6: Draw the circuit (or attach schematic)

Step 7: Implement and test the circuit. Draw the light segment pattern for each input.

Did the outputs in Step 7 match the truth table in Step 5? Yes___, No_____

If your answer is yes, you are done. Show it to your TA and have him check off your lab.

If your answer is no, debug your logic and circuit until they match, and then have your TA check off your lab.