EE 1315 DIGITAL LOGIC LAB

EE Dept, UMD

EXPERIMENT # 6: Implementation of Boolean Functions Using Multiplexers and Decoders

This lab involves design of standard Boolean functions using multiplexers and decoders. Before implementation, carefully study the operation of 8-to-1 multiplexers and 3-to-8 Decoders. The multiplexers (M8_1E) and decoders (D3_8E) available in the Xilinx ISE have an enable pin that must be set to logic high (vcc in the Xilinx library) for proper operation. To aid in understanding how component symbols in Xilinx ISE behave, the following step can be taken:

Place the component, in this case a M8_1E, on a schematic. Select the component by left clicking on it (it will become highlighted). Then with the symbol selected **Right click** and select **Object Properties**. A new window will appear as seen in Figure 1. From this window click **Symbol Info**. This will open a new help window seen in Figure 2. This has important information such as the truth table for the component. This can be done for any symbol in the Xilinx library.

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	Name InstName SymbolName Level	Value XUXL1 m8_Ie MXR_INX	8	Visible	New Edit Trats Delete	Understanding the SE Design Flow Norking with SF Report Underlay with SF Report Underlay with SF Report Underlay and SF Report Underlay and Section Section Section Section Section Section Section Therefore section Section	21 22 23 24 25 26 25 26 27 20						
	Libver VeriModel VhdlModel	Violation Image: Constraint of the constrain		Symbol Info	Separation playman and the mathematical final term of the mathematical field of the mathema	is an 8-to-1 multiplexe control of the select in w.	er with enable. When the nputs (52 : 50). The out	enable input (E) is High sut (O) reflects the sta	n, the MB_1E multiplexer choose to of the selected input as sh	ses ane data bit from eig own in the logic table. W			
						E 52 51				Inputs			Outputs
							51	50	07-00	0			
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	-												

Figure 1: Object Properties window

Figure 2: Symbol Info Window

Part A: Implement the following Boolean function using an 8-to-1 multiplexer and inverters (if necessary).

f(w,x,y,z) = w'y' + w'x'z + wx'y + wy'z'

Part B: Implement the following two functions using a single 3-to-8 decoder and some supporting gates.

g(x,y,z) = x'z + xz' + xyh(x,y,z) = x'z + xyz' + x'y'z'

Use the following table to assign the Scalar Ports to the sites on the FPGA board.

		Inp	Outputs				
Scalar Port	w	Х	Y	Z	F	G	н
Nexys I/O	SW0	SW1	SW2	SW3	LD0	LD1	LD2
Site	G18	H18	K18	K17	J14	J15	K15

EXPERIMENT #6 RESULTS

(Print out the following pages and bring with to the lab session)

Your Name: _____

Witnessed by Instructor or TA: _____

Date _____

Part A: Boolean function implementation using Mux

Express f(w,x,y,z) using minterms. $f(w,x,y,z) = \Sigma($

Fill in the minterm table and derive the circuit for each mux input.

	I ₀	I ₁	I ₂	I ₃	I_4	I ₅	I ₆	I ₇
w'	0	1	2	3	4	5	6	7
W	8	9	10	11	12	13	14	15

Show the circuit.

Build the circuit schematic in the Xilinx ISE. Fill in the truth table observed from the FPGA board.

W	X	у	Z	f
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1				
1				
1				
1				
1				
1				
1				
1				

Part B: Boolean function implementation using decoders

Find the minterms for the given functions g and h.

$$g(x,y,z) = \Sigma($$

h(x,y,z) = $\Sigma($

Design the circuit.

Build the circuit for the given functions g(x,y,z) and h(x,y,z) in Xilinx ISE and verify your circuit. Fill in the truth table observed from the FPGA implementation.

X	у	Z	b	h
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Have your TA verify your work.