EE 1315 DIGITAL LOGIC LAB

EE Dept, UMD

EXPERIMENT # 6: Implementation of Boolean Functions Using Multiplexers and Decoders

This lab involves design of standard Boolean functions using multiplexers and decoders. Before implementation, carefully study the operation of 8-to-1 multiplexers and 3-to-8 Decoders. The multiplexers (M8_1E) and decoders (D3_8E) available in the Xilinx ISE have an enable pin that must be set to logic high (vcc in the Xilinx library) for proper operation. To aid in understanding how component symbols in Xilinx ISE behave, the following step can be taken:

Place the component, in this case a M8_1E, on a schematic. Select the component by left clicking on it (it will become highlighted). Then with the symbol selected **Right click** and select **Object Properties**. A new window will appear as seen in Figure 1. From this window click **Symbol Info**. This will open a new help window seen in Figure 2. This has important information such as the truth table for the component. This can be done for any symbol in the Xilinx library.

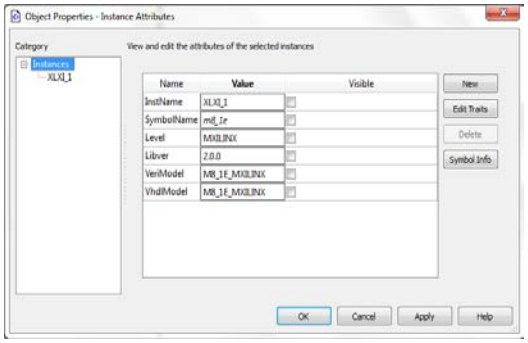

Figure 1: Object Properties window

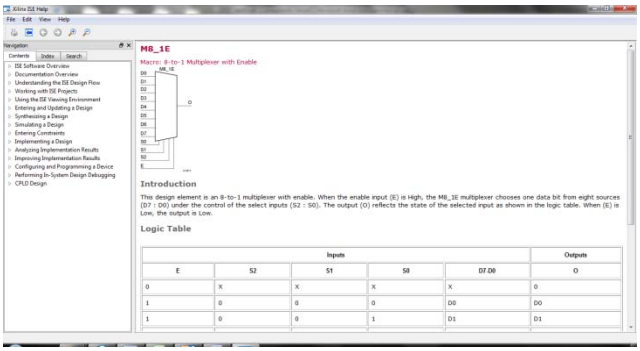

Figure 2: Symbol Info Window

Part A: Implement the following Boolean function using an 8-to-1 multiplexer and inverters (if necessary).

f(w,x,y,z) = w'y' + w'x'z + wx'y + wy'z'

Part B: Implement the following two functions using a single 3-to-8 decoder and some supporting gates.

g(x,y,z) =x'z + xz' + xy
h(x,y,z) = x'z + xyz' + x'y'z'

Use the following table to assign the Scalar Ports to the sites on the FPGA board.

	Inputs				Outputs		
Scalar Port	**W**	**X**	**Y**	**Z**	**F**	**G**	**H**
Nexys I/O	**SW0**	**SW1**	**SW2**	**SW3**	**LD0**	**LD1**	**LD2**
Site	**G18**	**H18**	**K18**	**K17**	**J14**	**J15**	**K15**

EXPERIMENT #6 RESULTS

(Print out the following pages and bring with to the lab session)

Your Name: _____

Witnessed by Instructor or TA: _____

Date _____

Part A: Boolean function implementation using Mux

Express f(w,x,y,z) using minterms.

f(w,x,y,z) = Σ(

Fill in the minterm table and derive the circuit for each mux input.

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
w'	0	1	2	3	4	5	6	7
w	8	9	10	11	12	13	14	15

Show the circuit.

Build the circuit schematic in the Xilinx ISE. Fill in the truth table observed from the FPGA board.

w	x	y	z	f
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1				
1				
1				
1				
1				
1				
1				
1				

Part B: Boolean function implementation using decoders

Find the minterms for the given functions g and h.

$g(x,y,z) = \Sigma($
$h(x,y,z) = \Sigma($

Design the circuit.

Build the circuit for the given functions g(x,y,z) and h(x,y,z) in Xilinx ISE and verify your circuit. Fill in the truth table observed from the FPGA implementation.

x	y	z	g	h
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Have your TA verify your work.