EE 1315: DIGITAL LOGIC LAB

EE Dept, UMD

EXPERIMENT # 7: Basic Latches

        Latches are primitive memory elements of sequential circuits that are used in building simple noise filtering circuits and flip-flops. This lab will explore the basic functionalities of latches using a SR-latch, a gated SR-latch, and a gated D-latch. Please notice during the experiment that the circuits are progressively more stable. Also, try to observe how latches provide a single bit memory.

        Since the latch circuits have feedbacks, their functions are dependent upon the past states as well as the present inputs, and the functions can no longer be expressed using a truth table. In a sequential circuit, the truth table must include the present and next states in addition to inputs and outputs to correctly express their functions. This type of table is referred to as a **state table** and used as a truth table for sequential logic circuits.

Part A: Build an SR-latch using a NAND circuit (also called NAND latch) given below
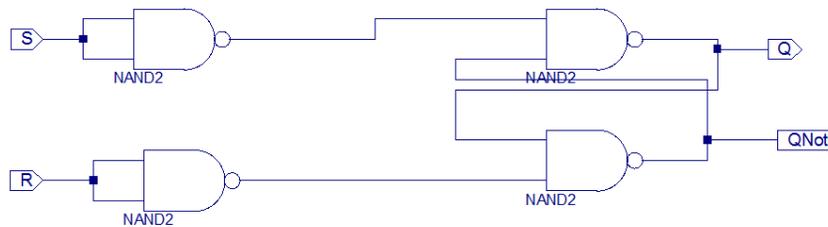
Find the state table using I/O on the Nexys 2 board, and record the observed values in the result section (make sure to have the TA check your circuit before continuing as it will be altered in the next step). Use the following site values for the Scalar Ports.

Scalar Port	S	R	Q	QNOT
Nexys I/O	SW0	SW1	LD0	LD1
Site	G18	H18	J14	J15

If you change from SR=11 to SR=00, it produces a so-called unknown state, that is, the state is determined based on the delay difference of the feedback lines that cannot be predicted. Check yourself by changing SR from 11 → 00 using input switches, and then observe the output states and record it in the result section.

A clock input will now be added to the circuit. This will be modeled by pressing one of the push-buttons on the Nexys 2 board. Because the push button is a mechanical switch, it produces so called a signal bouncing effect as shown in Fig 1. Therefore, the key-press needs to be de-bounced to convert the noisy button signal to a clean clock signal.

Fig 1. Signal bounce by a typical button release and press event.

A button debounce module has been created for your use to eliminate this problem. To add this module, please follow the steps provided below.

Step 1: Right-Click on the device in the **Design** window seen here and choose **Add Source**:
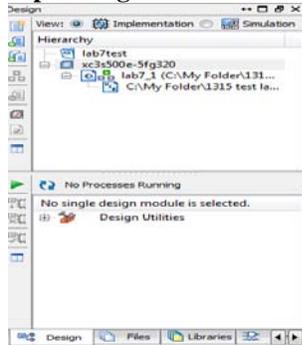
Step 2: Navigate to **C:\Xilinx\debounce\debounce.vhd** and select **Open**. A window should appear that indicates the successful addition of the module to your project. Click **OK**.

Step 3: Return to your schematic and add a symbol. With the category **All Symbols** selected, type **btn** in the symbol name filter box. You will see the symbol **btn_debounce** remains in the selection box. Choose it and place it on your schematic. Continue to part B.

Part B: Modify the circuit in Part A to a gated SR-latch. For wiring, the ISE requires a net name for each internal connection. Connect the circuit as seen below. You may receive an error message stating: "Only one net is allowed to connect to a pin." This just requires that the connection be made in the middle of the wire, not on the pin (note the connection symbol where the btn_debounce connects to the 2 **NAND** gates.
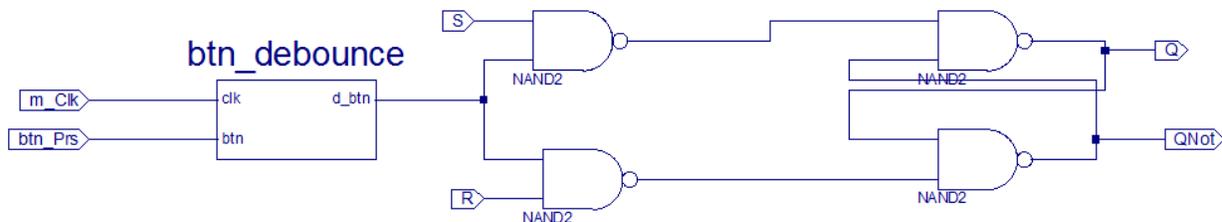
Note the additional inputs on the clock module. In this example the ports have been named m_Clk and btn_Prs, but you can name them anything you like. These ports will need to be assigned in the UCF. To accomplish this, navigate to **User Constraints->I/O Pin Planning (Plan Ahead)**. The RTL design editor will open as usual. You should by now be familiar with assigning ports to sites on the board. Set the btn_Prs I/O port to the BTN0 of the push buttons on the Nexys 2 board (B18, D18, E18, or H13). Now assign the m_Clk I/O port to B8 (this is the site for the board's internal 50 MHz oscillator) and **S**ave (see the following table). You may now run the **Synthesize**, **Implement Design**, and **Generate Programming File** in the normal way.

Scalar Port	S	R	m_Clk	btn_Prs	Q	QNOT
Nexys I/O	SW0	SW1	50MHz	BTN0	LD0	LD1
Site	G18	H18	B8	B18	J14	J15

Scalar Port Assignment Table

The clock input adds more control on Q and creates a true memory element. Find the state table using the boards I/O, and then record the results in the result section. Note that to change outputs on the FPGA board, the push button labeled BTN0 must be pressed and the input switches must be adjusted. Again be sure to show your TA before continuing.

Part C: Modify the circuit in Part B to a gated D-latch as shown below. You may again receive an error message stating: "Only one net is allowed to connect to a pin." This just requires that connections be made in the middle of the wire, not on the pin.
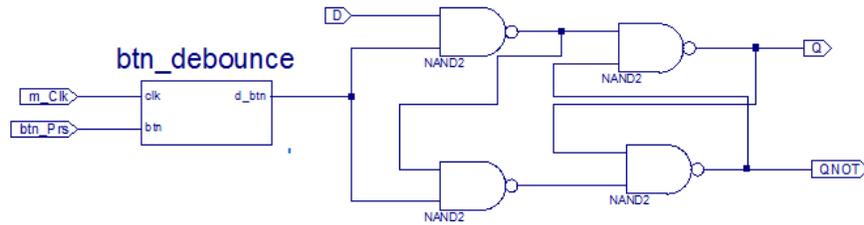
Notice that the clock is more effectively used in this circuit. Find the state table using the Board's I/O and then record the results in the result section. Also since the S and R inputs have been replaced with a single D input, the UCF will need to be changed before you can test the circuit. Use the following table to set the Scalar Ports.

Scalar Port	D	m_Clk	btn_Prs	Q	QNOT
Nexys I/O	SW0	50MHz	BTN0	LD0	LD1
Site	G18	B8	B18	J14	J15

Scalar Port Sites for gated D-latch

EXPERIMENT #7 RESULTS
(Print out this section and bring with to the lab session)

Your Name: _____

Witnessed by Instructor or TA: _____

Date _____

Have your TA verify the results after completion of each part.

Part A: State Table for SR-latch

Input		Present State	Next State	
S	R	Q	Q+	Q'+
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Mark the not-allowed cases if you could notice them.

Your observation on change of SR from 11 → 00:

Part B: State Table for gated SR-latch

Inputs and Present States				Next States	
S	R	Q	C	Q+	Q'+
0	0	0	0		
0	0	1	0		
0	1	0	0		
0	1	1	0		
1	0	0	0		
1	0	1	0		
1	1	0	0		
1	1	1	0		
0	0	0	1		
0	0	1	1		
0	1	0	1		
0	1	1	1		
1	0	0	1		
1	0	1	1		
1	1	0	1		
1	1	1	1		

Mark the not-allowed cases and explain why.

Part C: State Table for gated D-latch

Input		Present State	Next State	
C	D	Q	Q+	Q'+
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Mark the not-allowed cases if you found them. Explain why it is different from the S-R latches.