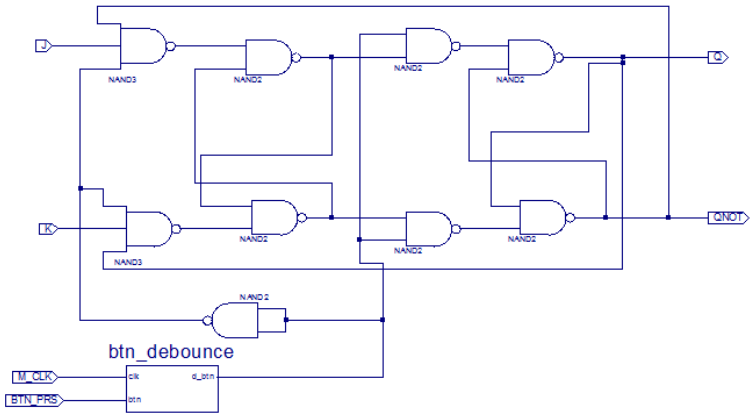
EE 1315 DIGITAL LOGIC LAB

EE Dept, UMD

EXPERIMENT # 8: Master-Slave Flip-Flop

In this lab, you will investigate the behavior of a master-slave flip-flop (FF). Master-slave FFs eliminate the direct pass-through conditions of latches by cascading two latches to lock the output signal at the opposite gated signal (clock). That is, if one of the latches is in a gated state (pass through state), the other latch is in a hold state creating a synchronization effect on a clock edge.

Build the JK Master-Slave FF circuit given below using the schematic tools. You will need a clock module, seven nand2's, and two nand3's. Remember to **right click** on the project in the **design** tab and choose **add module**. Navigate to **C:\Xilinx\debounce\debounce.vhd** and select **Open**. A window should appear that indicates the successful addition of the module to your project. Click **OK**.



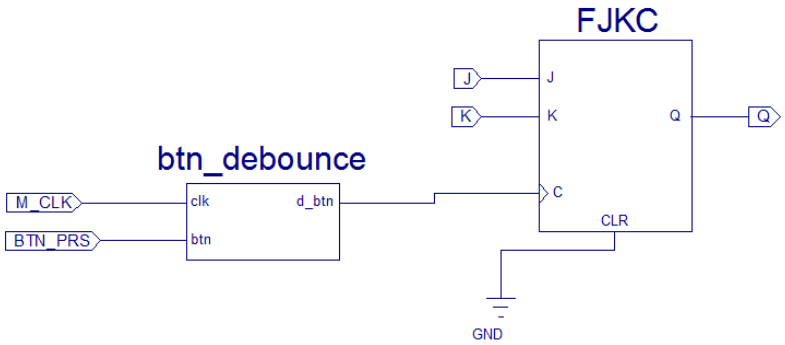
After the circuit has been constructed in Xilinx ISE, set the Scalar Ports as indicated in the following table.

	Inputs				Outputs	
Scalar Port	**J**	**K**	**M_CLK**	**BTN_PRS**	**Q**	**QNOT**
Site	**G18**	**H18**	**B8**	**B18**	**J14**	**J15**

Complete the first table in the results section. Do this by setting each input (J and K) when the output is specified as a 0 or 1 and press the button (BTN0) to "tick" the clock. Show your TA the working circuit.

Part 2: Test the JK-FF provided by the Xilinx ISE library

Xilinx ISE has a J-K Flip Flop symbol that is available for your use. For this part, you may edit the schematic you have already created, but it may be completed more easily if a new project (perhaps called Lab8_part2) is created. Click on **Add Symbol** and either navigate to the **Flip_Flop** category and choose the **fjkc** symbol or use the symbol filter. Add the symbol to your schematic, right click and choose **ObjectPproperties -> Symbol Info** to learn about the behavior of the flip flop provided by Xilinx ISE. Note that there is an **Asynchronous Clear** pin on the flip flop that **MUST** be logic low (a zero) to operate properly. Create the following circuit in your new schematic.



Notice the **GND** component that will set the **CLR** pin to a zero. There is no QNOT supplied by the Xilinx ISE library, so it will be omitted from the output in this circuit. Use the values in the following table to set the Scalar Ports for your circuit.

	Inputs				Output
Scalar Port	**J**	**K**	**M_CLK**	**BTN_PRS**	**Q**
Site	**G18**	**H18**	**B8**	**B18**	**J14**

Check the outputs of the circuit and make sure that they are identical to those that were found in the first part of this lab. Show your TA the working circuit for a check-off of this lab.

EXPERIMENT #8 RESULTS

(Print following sheets and bring to lab session)

Your Name: _____

Witnessed by Instructor or TA: _____

Date _____

Record the data observed from Part 1.

Inputs		Present State	Next States	
J	K	Q	Q+	Q'+
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Since the Part 2 results should be the same as the Part 1, no need to separately record them but show the circuit and results to your TA.