# Department of Electrical Engineering
EE 1315: Digital Logic
LogiScan User Manual

What is LogiScan?

LogiScan is a USB-based digital-circuit testing tool designed for EE 1315 labs. It consists of an interface box and software that runs on a PC. The interface box is controlled from the PC through a USB connection and generates input test patterns for the input pins selected and PC-monitor displays for output pin values. LogiScan is capable of testing both combinatorial and synchronous sequential circuits up to six inputs and outputs.
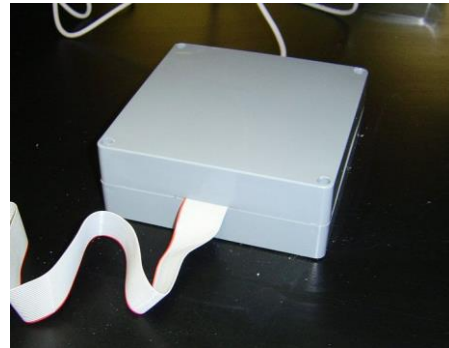
The USB port of the LogiScan interface box must be plugged into a Lab PC before you run the LogiScan software.

Pin-out diagram of the 24 pin in-line Connector

The most important information that students need to know before using LogiScan is the pin-outs of the 24-pin ribbon-cable connector of the interface box. This connector shown in Figure 1 provides all necessary interfaces between your breadboard and the LogiScan interface. Please note where the pin #1 and #24 is in relation to mark and the side of ribbon cable. Figure 1 is the top view of the connector, and pin #1 is located at left top of the connector and it is marked "1".
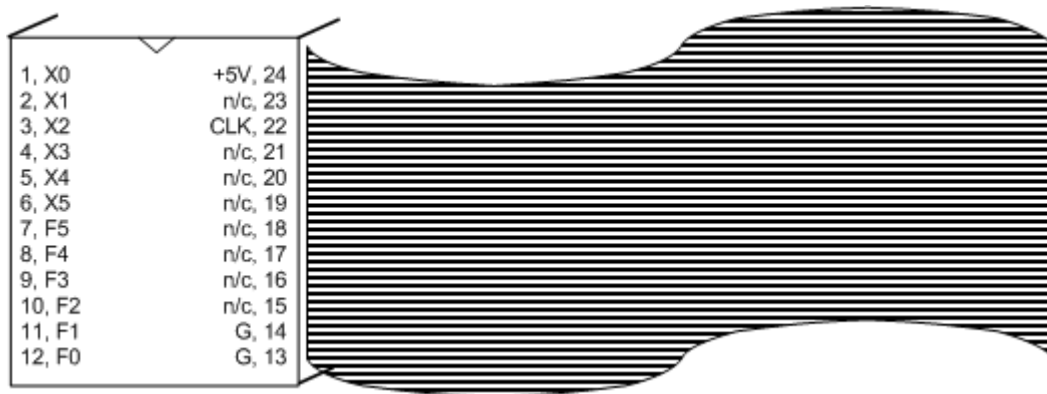

1, X0	+5V, 24
2, X1	n/c, 23
3, X2	CLK, 22
4, X3	n/c, 21
5, X4	n/c, 20
6, X5	n/c, 19
7, F5	n/c, 18
8, F4	n/c, 17
9, F3	n/c, 16
10, F2	n/c, 15
11, F1	G, 14
12, F0	G, 13

Figure 1: Pin-outs of the LogiScan 24pin inline connector

Pins 1,2,…,6: X0, X1, ..., X5
LogiScan generates logic signals and then sends them out to pins 1 to 6, so they must be connected to the inputs of your circuit. The bit pattern of logic-0 and logic-1 (0 or 5Volts) can be controlled by clicking the red square buttons or through an input table.

Pins 12,11,…,7: F0, F1, ..., F5
These pins must be connected to the outputs of your circuit. The LogiScan interface reads these pins and then displays them on the PC screen. Note that F0 starts from pin 12 and then assigned in a descending order, i.e., 11, 10, 9, etc. The LED images of light-on and light-off correspond to logics 1 and 0, respectively.

Pin 24: +5V
This pin provides +5V power supply and should be connected to Vcc of your circuit.

Pin 13, 14: G
Two pins, #13 and #14, provide GND (0V) and one of them should be connected to the GND pin of your TTL chip.

Pin 22: CLK
This pin provides a clock signal for running sequential logic circuits. The clock cycle can be programmed using the Clock menu and controlled by the Stop and Start item in the Clock menu.

Controlling signals using the LogiScan software

The LogiScan software runs when you double-click on the icon

LogiScan.exe

If the software does not open up the main window as shown in Figure 2, you may need to pull out and then plug the USB connector back in to PC to wake up the USB device driver. Another option would be a reset to bring back the device driver to recognize the board. If such actions do not fix the problem, please report the problem to the EE shop or lab coordinator
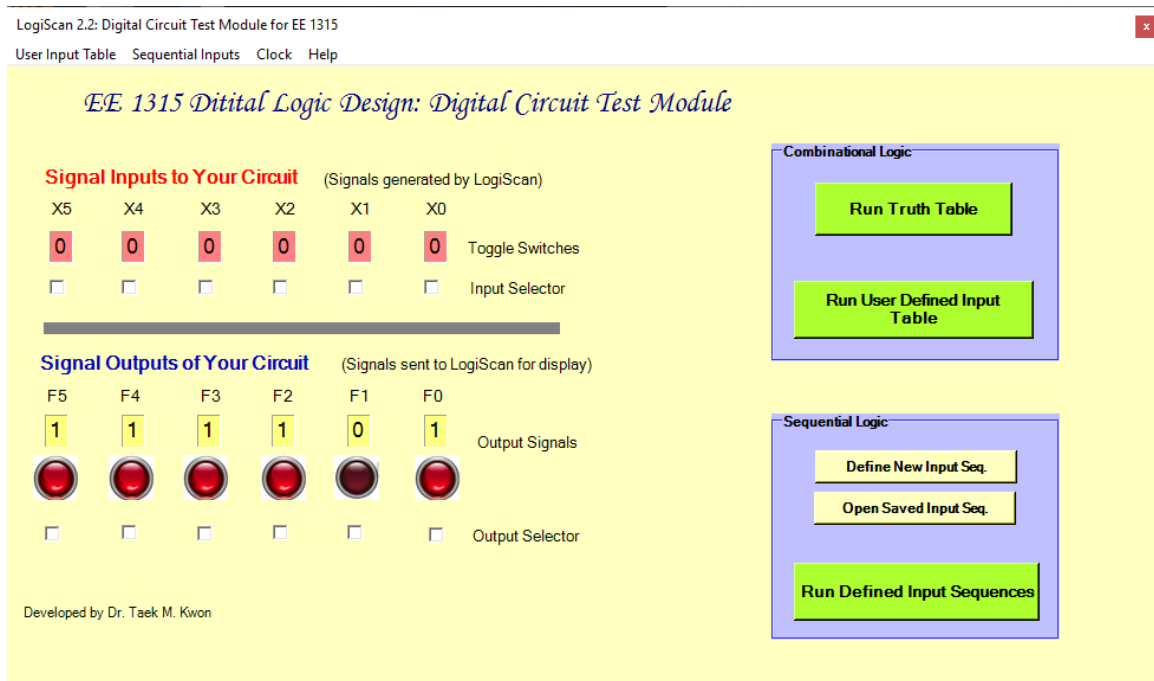

Figure 2: LogiScan screen

LogiScan produces +5V for logic-1 and 0V for logic-0 and sends out the voltage signals to pins X0 through X5. **The red squares under the labels X0-X5 toggle between 0 and 1 when you click on it using the left mouse button**, which then immediately sends the corresponding voltages (0V or +5V) to the corresponding pins. **The check boxes under the red squares are used to define used (or connected) inputs for generating a truth table.**

The outputs of your circuit should be connect to pins F0-F5. The "1" or "0" in the yellow boxes under the label "**Signal Outputs of Your Circuit**" is the real-time read-out results corresponding to +5V or 0V on the respective pin. The check boxes under the yellow boxes are used to select outputs for generating a truth table of your circuit.

Initial Loopback Test

This is a simple loopback test that shows if the LogiScan interface box and software are working or not. Connect X0 to F0 and X1 to F1 as shown in Figure 3. This connection simply shows the test patterns generated from X0 and X1 at F0 and F1. Toggle the signals in X0 and X1 by pressing the toggle switch buttons (red box) and then check if that signal matches with the output displayed in the corresponding yellow boxes and LED images. If the patterns of input do not match with the output, it indicates a faulty condition and requires a repair. If the input and output patterns match, you can move on to other positions to test them in a similar manner.
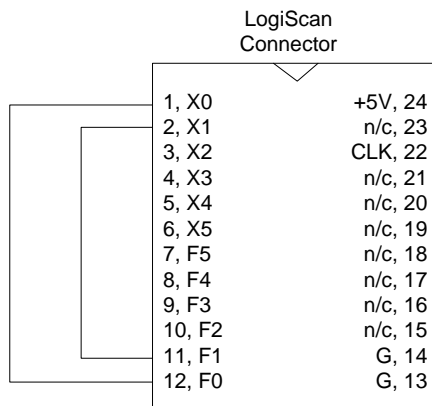
```
                        LogiScan
                        Connector

            1, X0              +5V, 24
            2, X1              n/c, 23
            3, X2              CLK, 22
            4, X3              n/c, 21
            5, X4              n/c, 20
            6, X5              n/c, 19
            7, F5              n/c, 18
            8, F4              n/c, 17
            9, F3              n/c, 16
            10, F2             n/c, 15
            11, F1               G, 14
            12, F0               G, 13
```

Figure 3: Direct loopback test

Combinational Logic: A Walk-Through Example

This example illustrates how to connect and test an OR gate using a 74LS32 chip. A 74x32 chip includes four 2-input OR gates, and we will use only the first one of the four. Using your breadboard, connect the two inputs of the first OR gate to X0 and X1 and the output of the OR gate to F0, and also Vcc to +5V and GND to G, as shown in the connection diagram in Figure 4.
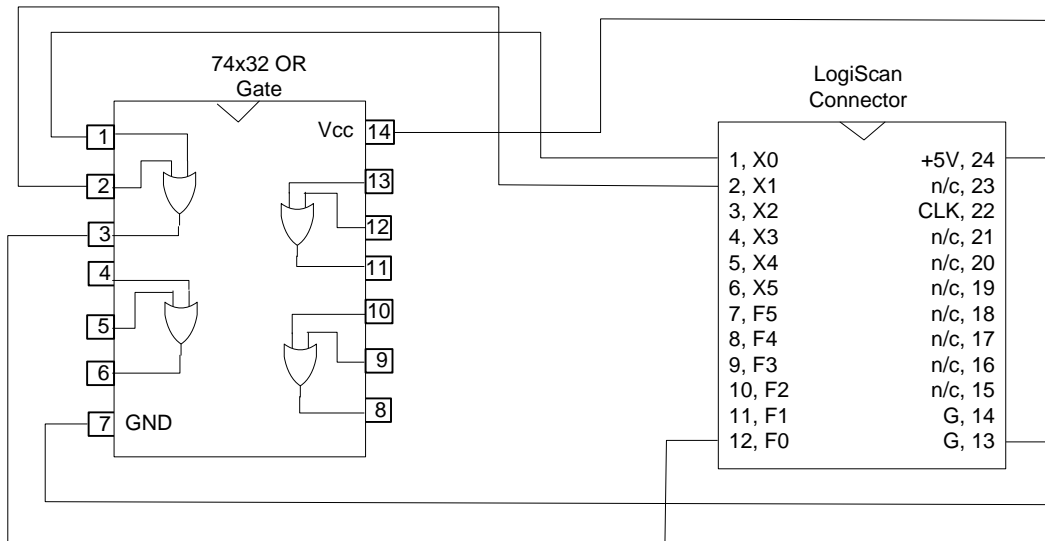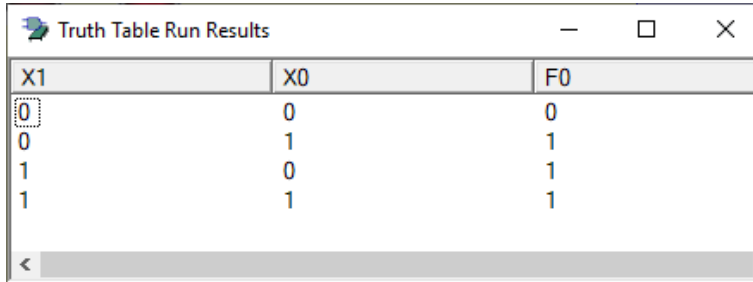

Figure 4: Connection diagram of an OR gate test circuit

Next, using the LogiScan screen toggle the signals of X0 and X1 by clicking on the corresponding red squares and observe the output, F0. The LED images will also show ON for logic 1 and OFF for logic 0.

By manually changing X0 and X1 values, you should be able to obtain the following OR truth table.

X1	X0	F0
0	0	0
0	1	1
1	0	1
1	1	1

Now, check mark on X0, X1, and F0, and then click the "**Run Truth Table**" button. You should be able to see a pop-up window that contains the circuit's truth table shown in Figure 5.
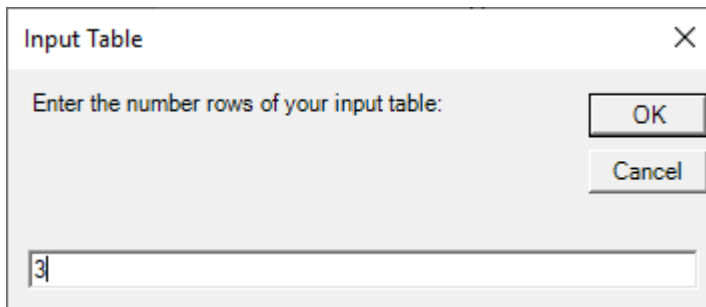

X1	X0	F0
0	0	0
0	1	1
1	0	1
1	1	1

Figure 5: A popup window that shows the truth table of the OR circuit

Partial input combinational logic tests

When a combinational circuit has many inputs, often only a part of input combinations need to be tested. In such a case, you need to build your own input test patterns. To define the input test patterns, select the menu item: "**User Input Table**" → "**Build New One**". For illustration, above OR gate connection is used. Suppose that you only wish to test three input patterns then "3" is entered in the "**Input Table**" dialog (Figure 6), which brings out the "**User Defined Input Table**" window (Figure 7).

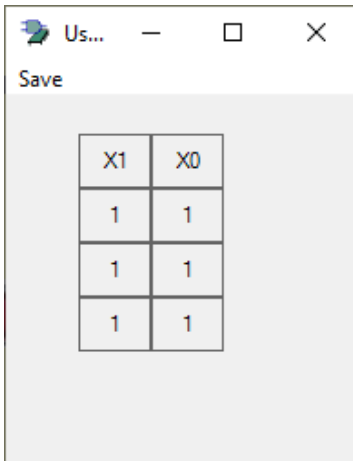**Figure 6: Number of entries in the Input Table dialog**

Figure 7: User defined input table. You can design your input patterns by toggling the input bits.

The default values the **User Defined Input Table** are all logic 1s and the desired input patterns are generated by pressing left mouse button on the input value which toggles between 0 and 1. Various input patterns can be easily created by toggling the input bits. For this example, the input patterns are created as shown Figure 8.
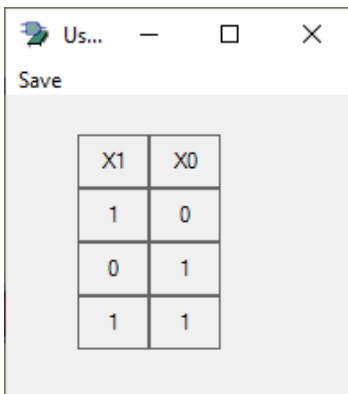

Figure 8: User generated input patterns

After creating the input table, make sure to save it by clicking the menu "**Save Table and Exit" under Save menu** or by answering **"Yes"** before closing the window. It is important to save the inputs defined because the truth table is run based on the saved input patterns.

Now, run the circuit using the "**Run User Defined Input Table**" button. The final output of this example consists of three rows and is shown in Figure 9.

Figure 9: Truth table output for the user defined input patterns

See next page for a walkthrough example of a synchronous sequential logic circuit.

Synchronous Sequential Logic

In a sequential circuit, the output is no longer just a function of the present input signals but also a function of the past inputs. More specifically, a circuit may produce a different output even if the present inputs are the same but if the past inputs were different. It also uses a clock to differentiate the timing of signals from past to present.

Testing a sequential logic circuit requires the following steps.
- Connect your circuit to LogiScan, i.e., inputs of your circuit to X0-X5 and outputs of your circuit to F0-F5.
- Connect the clock input of your circuit to the LogiScan Clock pin (pin 22)
- Select the check boxes for the inputs and outputs you connected.
- Next define the input sequences using the "**Define New Input Seq.**" button in the Sequential Logic box (purple box) or from the menu.
- Make sure to save the input sequence by clicking on the **Save** button. Remember that the run function uses only the saved input sequences. If saving is done, you can now close the **Input Sequence** window.
- Run your circuit by clicking on the "**Run Defined Input Sequences**" button.
- The run result will appear on a new popup window and you should analyze the results to check if the output sequences are correct. If it is not, you will need to correct your circuit.

Walk-Through Example: D-FF

Let's test the functionality of a D-FF output. 74x74 has two D-FFs, and we will use only one of them. The output sequence expected is one clock cycle delayed from the input sequence.

Step 1) Make connections on your breadboard as shown in Figure 10. Notice that the input "1D" is connected to X0, the output "1Q" is connected to F1, and "1CLK" to CLK (pin 22). CLR* and PRE* are inverted logic, and both are connected to +5V (Logic 1 = no preset, no clear).
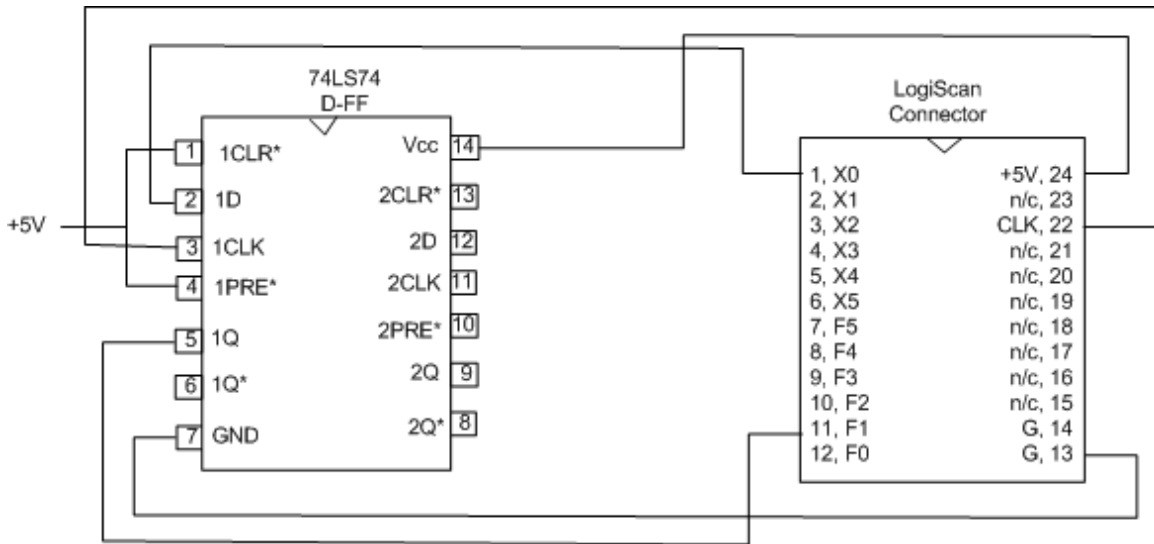
Figure 10: D-FF test circuit

Step 2) Since X0 is used as the circuit's input sequence and F1 is used as the circuit's output sequence, place check marks on X0 and F1 as shown below.

Step 3) Define the input sequence.
Click on the "**Define New Input Seq.**" which would bring up the following window.
Enter 20 and then click **OK** as shown below.
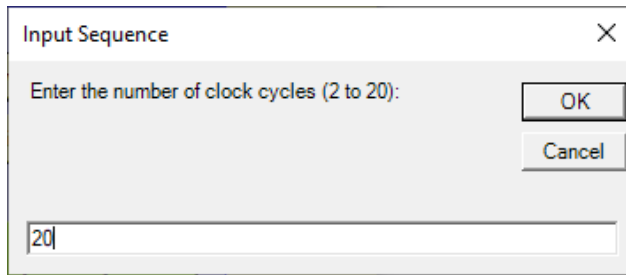
Next, you will see a popup window for editing input sequence. Choose the Rising edge radio button since 74LS74 is synchronized to the rising edges of its clock and then toggle the values of X0 to create your own sequence as shown in Figure 11.
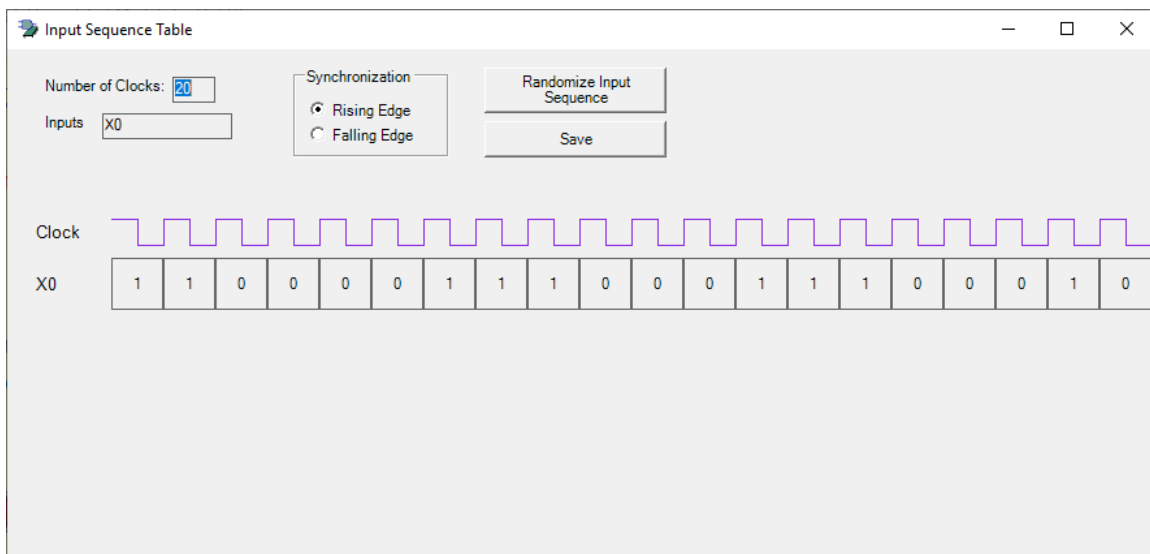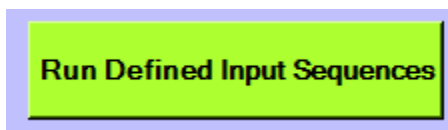

Figure 11: Input sequence edit

Next step is to save the generated sequence using the **Save** button. Click the **Save** button and then OK to close the Input Sequence Table. Please remember that the saved sequence is the one that the LogiScan uses. If you want to see the saved sequence again, press the "Open Saved Input Seq." button.

Step 4) Run the sequential circuit by clicking on the "**Run Defined Input Sequences**" button. Then, a Run Results window will popup.

Step 5) Analyze the run results, i.e. study the output sequence

The screen capture of the Run results window is shown in Figure 12. Notice that all input values appear in the output with one clock delay, synchronized at rising edges. This is exactly how a D-FF is supposed to work.
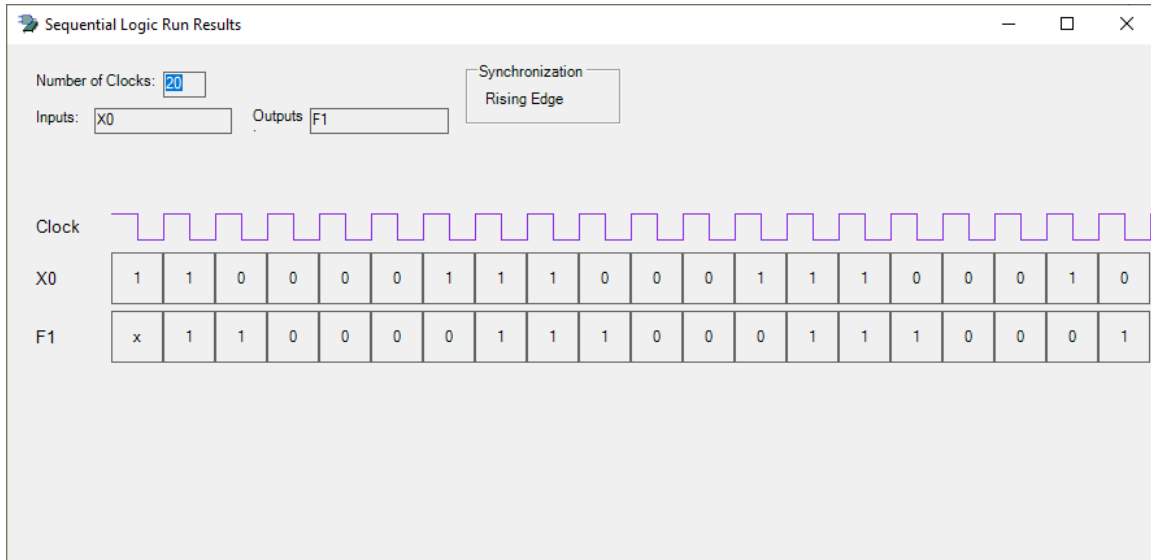

Figure 12: Finial run output of the D-ff circuit

Now, you have successfully completed a walk-through example of a sequential circuit. A similar procedure should be used for testing your future sequential circuits.

*Never disconnect the USB port while LogiScan is running.

Remarks

In summary, LogiScan provides six programmable ports for input patterns and six output ports for display. Any combinational or synchronous sequential logic circuits having less than six inputs and outputs can be tested by using the steps shown in the above walk-through examples. LogiScan essentially works as a logic analyzer simplified for small digital circuits.

One of the important things to remember is to save the input patterns or input sequence after you created one. LogiScan only uses the saved input patterns or sequences to generate the outputs of the test circuit. Once it is saved, the data is in the memory and you can review the data by clicking on the menu "**Sequential Inputs→Open Existing**" for a sequence input and the menu item "**User Input Table→Open Existing**" for a combinational logic.

LogiScan was developed by Dr. Taek M. Kwon in the Electrical Engineering Department at UMD. If you are experiencing problems and the problem was not resolved through your TA or instructor, please contact Dr. Taek Kwon.