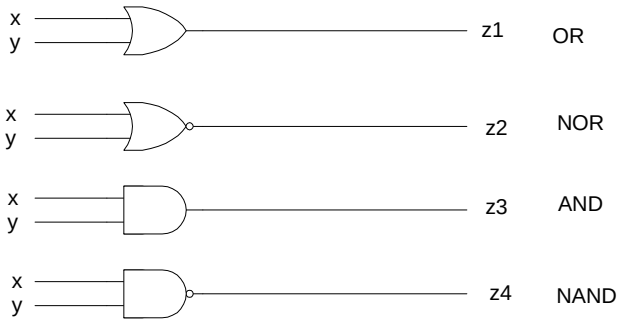
ECE 1315 DIGITAL LOGIC DESIGN

ECE Dept, UMD
Jan 24, Tuesday, 2006

EXPERIMENT # 1: Logic building blocks

The main objective of this experiment is to let you familiarize with the lab equipment and learn about the operation of the fundamental combinational logic elements, **AND**, **OR**, **NAND, and NOR** gates in this experiment. The TA will explain how to use the LogiScan, breadboard, and TTL chips.

For the experiment, find the corresponding IC chip and wire the circuit shown in the following diagram on your breadboard. The TTL chips you need to use are 74LS00, 74LS02, 74LS08, and 74LS32. Wire one gate at a time and test the functionality.



Remember to connect the power supply **Vcc** and **GND** lines to the TTL chip. Also, remember that any outputs of the gate cannot be connected together. If you do so, it causes a short circuit and will destroy the chip or the LogiScan interface.
For learning the gate and pin-out information, please use the following web page.
http://www.d.umn.edu/~tkwon/course/1315/lab/TTLPinout/pinouts.html

It is always a good idea to test if the LogiScan pins are working correctly or not. You can test it by simply connecting single wire from a pin X# to a pin F# where # is one of 0-5, i.e., connect one output to one input. After the single wire connection, if you click on the red square under the X# from the LogiScan software, the same logic should show under the square F#. If the logic between the input and output does not match, you should report it to TA and get it fixed.

Connecting LogiScan

Part 1: One chip at a time
Plug in one chip at a time for each gate function given. Connect the inputs x and y of the gate to the X0 and X1 pin of the LogiScan, and the output z# to the F0 pin of the LogiScan. You then should find out the function (input-output relation) of each gate by toggling X0 and X1 (by click on the corresponding red square of the LogiScan software) and record your observation on the results sheet.

Part 2: All chips at a time
Plug in all four chips on the breadboard, and tie all x's together to one line and all y's together to another line. Then connect the x line to X0 and the y line to X1. Connect the gate outputs, z1, z2, z3, z4 to the F0, F1, F2, and F3 pins of the LogiScan, respectively. Run truth table by clicking on the "Run Truth Table" button. Check if this result matches with the results of Part 1, if so use this setup to check off your lab.

***Print the Results page and bring it to the lab

EXPERIMENT #1 RESULTS

Witnessed by :

Date _____

Recorded Truth Table

x	y	z1 (OR)	z2 (NOR)	z3 (AND)	z4 (NAND)
		IC#:	IC#:	IC#:	IC#:
0	0				
0	1				
1	0				
1	1				

1. Which pairs of gates have inverting relations according to the truth table above?

2. Write an algebraic equation for each type of gate using the inputs x and y (refer to the web pages of the pin-outs, or textbook, or ask TA)

OR:

NOR:

AND:

NAND: