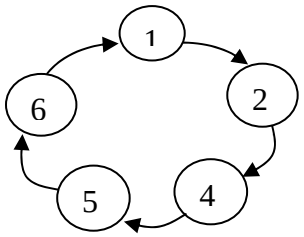
ECE 1315 DIGITAL LOGIC DESIGN

ECE Dept, UMD
Apr 11, Tuesday, 2006

EXPERIMENT # 10: Arbitrary Number Sequence

Design a synchronous counter that counts a sequence of three-bit numbers using T-ffs given by

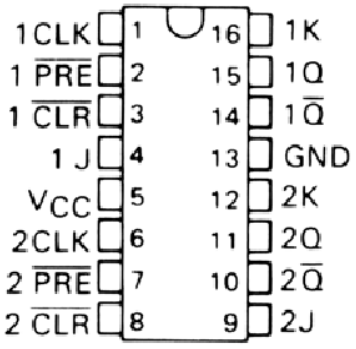


For the T-ff function, use 74LS76 (JK-ff) by connecting the J and K inputs together. 74LS76 chips contain two JK-ffs, and each JK-ff has Preset and Clear control inputs that work active low, so both pairs of Preset and Clear should be tied to +5V for normal FF operations. Also, be careful in connecting Vcc and GND. **Vcc is at Pin 5 and GND is at Pin 13 in 74LS76.** Since the states are the outputs of your circuit (counter), connect the three states to LogiScan F0, F1 and F2, and test the counter.

Steps

1. Design the counter by following the result section.
2. Run your circuit by connecting the outputs to LogiScan F0, F1 and F2.
3. From the Clock menu of the LogiScan, click on the item "Clock Period" and set the period to slow enough such as 500ms or 1000ms to be able to see the change of states on the LogiScan F0-F2 display boxes. We will refer to this clock as the free-running clock in the future. Then, click on the "Start" under the Clock menu to start the free-running clock. The free running clock is generated on the LogiScan clock output. If your circuit works correctly, you should be able to see the changes of number sequence that matches the state diagram.
4. Don't forget to stop the free-running clock after the testing is done.

74LS76 Pin Outs



EXPERIMENT #10 RESULTS

Your Name: _____

Witnessed by Instructor or TA: _____

Date _____

Show your design process.

Step 1) State/Excitation Table (State Table with T inputs)

Step 2) FF Input Equations

Step 3) Verification of State Diagram and Make Correction If Necessary, i.e, redraw the state diagram after the don't care terms are fixed and check for orphan loops

Step 4) Final Circuit Diagram

Step 5) Observed the Counter Patterns from the LogiScan Using Free- Running Clock