

# ECE 1315 DIGITAL LOGIC DESIGN

ECE Dept, UMD  
April 18, Tuesday, 2006

## EXPERIMENT # 11: Synchronous Sequence Detector

**Design and build a synchronous sequence detector that detects a bit-pattern “1010” using JK-ffs (74LS76). Please follow the steps provided in the result section.**

Note: The 74LS76 chip contains two JK-ffs, and each JK-ff has Preset and Clear control inputs that work active low so both pairs of Preset and Clear should be tied to a high level for normal operations. Please remember that the pin locations of Vcc and GND of 74LS76 are in odd places. See the pin outs of 74LS76 shown below. The clock inputs should be connected to the LogiScan “Clock” (pin 22) as before. When you debug the circuit, it is also a good idea to display the state outputs in the LogiScan.

74LS76 Pin Outs

1CLK	1	16	1K
1PRE'	2	15	1Q
1CLR'	3	14	1Q'
1J	4	13	GND
Vcc	5	12	2K
2CLK	6	10	2Q
2PRE'	7	11	2Q'
1CLR	8	9	2J

## **EXPERIMENT #11 RESULTS**

Your Name: \_\_\_\_\_

Witnessed by Instructor or TA: \_\_\_\_\_

Date \_\_\_\_\_

Show your design process.

**Step 1) Derive the State Diagram for “1010” sequence detector**

**Step 2) Derive the State Excitation Table**

**Step 3) Derive the FF Input Equations and the Output Equation based on the State Excitation Table**

**Step 4) Draw the Final Circuit Diagram**

**Step 5) Bild the Circuit**

**Step 6) Design and generate a desired test Input Pattern that can thoroughly test your circuit**

Test Input Sequence Pattern:

**Step 7) Run your circuit using LogiScan and record your test input sequence and the output results. If the sequence detector works correctly, have your TA approve the result.**