ECE 1315 DIGITAL LOGIC DESIGN

ECE Dept, UMD
Feb 14, Tuesday

EXPERIMENT # 4: Combinational logic application design

Combinational logic can be designed by following a standard design procedure as follows:

1. State the problem
2. Determine the required number of input and output variables
3. Assign the input and output variables to letter symbols
4. Derive the truth table
5. Simplify the function
6. Draw the circuit using gates
7. Implement and test the circuit

Given problem: Design and implement a two-bit signed adder (2's complement arithmetic) with an overflow output. For the overflow bit (V), use the overflow detection rule you learned in the class, i.e., an addition overflows if the signs of the addends are the same, but the sign of the sum is different from the addends' sign.

EXPERIMENT #4 RESULTS

Your Name: _____

Witnessed by

Instructor or TA: _____

Date _____

Step 1: State the problem

Step 2: Determine the number of required inputs and outputs
No of inputs: _____
No of outputs: _____

Step 3: Assign the input and output variables to letter symbols

```
        X1 X0
  +     Y1 Y0
-------------------
  V     S1  S0
```

where V is the overflow bit that indicates an overflow error. Each of the symbols X0, X1, Y0, Y1, S0, and S1, denotes a single bit.

Step 4: Construct the truth table of the given problem. Use the binary arithmetic.

Input				**Output**		
X1	**X0**	**Y1**	**Y0**	**S1**	**S0**	**V**
0	0	0	0	0	0	0
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1	1	0	1
0	1	1	0			
0	1	1	1			
1						
1						
1						
1						
1						
1						
1						
1	1	1	1	1	1	0

Step 5: Simplify the function. Remember to use XOR gates if necessary. It can reduce gate counts.

Step 6: Draw the circuit

Step 7: Implement and test the circuit

Input				Output		
X1	**X0**	**Y1**	**Y0**	**S1**	**S0**	**V**
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1						
1						
1						
1						
1						
1						
1						
1						

Did the truth table in Step 7 match the truth table in Step 5? Yes___, No____
If your answer is yes, you are done. Show it to your TA and have him check off.
If your answer is no, debug your logic and circuit until they match, and then have your TA check off.