# ECE 1315 DIGITAL LOGIC DESIGN 

## ECE Dept, UMD

Feb 21, Tuesday, 2006

## EXPERIMENT \# 5: Code Converter Design

Combinational logic can be designed by following a standard design procedure as you experienced in Experiment \#4. Another combinational logic problem is given for this week for designing the circuit using a minimum number of chips.

1. State the problem
2. Determine the required number of input and output variables
3. Assign the input and output variables to letter symbols
4. Derive the truth table
5. Simplify the function to use a minimum number of chips
6. Draw the circuit using gates
7. Implement and test the circuit

Given problem: Design a code converter that converts from a BCD (Binary Coded Decimal) to a 7536' code using a minimum number of chips. Both BCD and 7536' codes are used to express decimal digits 0-9, and thus they only use 10 patterns out of the $\mathbf{1 6}$ available patterns from the four bit combination. The unused bit patterns can be treated as don't care minterms. The code conversion table is given below:

| Decimal <br> digit | BCD <br> Code | $7536^{\prime}$ <br> Code |
| :--- | :--- | :--- |
| $\mathbf{0}$ | 0000 | 0000 |
| 1 | 0001 | 1001 |
| 2 | 0010 | 0111 |
| 3 | 0011 | 0010 |
| 4 | 0100 | 1011 |
| 5 | 0101 | 0100 |
| 6 | 0110 | 1101 |
| 7 | 0111 | 1000 |
| 8 | 1000 | $\mathbf{0 1 1 0}$ |
| 9 | 1001 | 1111 |

Notice that the 7536' code has a complemented symmetric relation, i.e., 5-9 codes are obtained by complementing 4-0. This type of code is called a self-complementing code and helps error detection.

## EXPERIMENT \#5 RESULTS

Your Name: $\qquad$

Witnessed by
Instructor or TA: $\qquad$
Date $\qquad$

Step 1: State the problem

Step 2: Determine the number of required inputs and outputs
No of inputs: $\qquad$
No of outputs: $\qquad$

Step 3: Assign the input and output variables to letter symbols

Step 4: Derive the truth table

| Input |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mid$ |  |  |  | Output |  |  |  |
| 0 | 0 | 0 | 0 |  |  |  |  |
| 0 | 0 | 0 | 1 |  |  |  |  |
| 0 | 0 | 1 | 0 |  |  |  |  |
| 0 | 0 | 1 | 1 |  |  |  |  |
| 0 | 1 | 0 | 0 |  |  |  |  |
| 0 | 1 | 0 | 1 |  |  |  |  |
| 0 | 1 | 1 | 0 |  |  |  |  |
| 0 | 1 | 1 | 1 |  |  |  |  |
| 1 |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |

Step 5: Simplify the output functions using K-maps.

Step 6: Draw the circuit. K-map gives you only minimization at the level of the minimum number of literals. For the actual implementation, you should minimize the circuit at the chip or gate level, especially for the circuits with multiple outputs like this lab. For this lab, design the circuit to use a minimum number of chips.

Step 7: Implement and test your circuit. For testing, try both the "Run Truth Table" and "User Defined Input Table". Which one should you use if the circuit contains many input variables and don't-care terms? Fill in the table below according to the outputs of your circuit.

| Input |  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :---: |
|  |  |  |  |  | Output |  |  |  |
| 0 |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |  |

