ECE 1315 DIGITAL LOGIC DESIGN

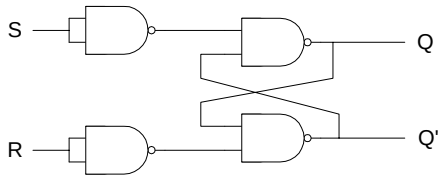
ECE Dept, UMD
Mar 21, Tuesday, 2006

EXPERIMENT # 7: Sequential Circuit: Basic Latches

Latches are primitive memory elements of sequential circuits that are used in building simple noise filtering circuits and flip-flops. This lab will explore the basic functionalities of latches using a SR-latch, a gated SR-latch, and a gated D-latch. Please notice during the experiment that the circuits are progressively more stable. Also, try to observe how latches provide a single bit memory.

Since the latch circuits have feedbacks, their functions are dependent upon the past states as well as the present inputs, and the functions can no longer be expressed using a conventional truth table. In a sequential circuit, the truth table must include the present and next states in addition to inputs and outputs to correctly express their functions. This type of table is referred to as a state table and used as a truth table for sequential logic circuits.

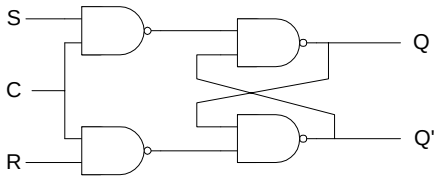
Part A: Build a SR-latch using a NAND circuit (also called NAND latch) given below



Find the state table using LogiScan, and record the observed values in the result section.

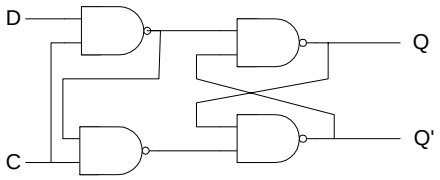
If you change from SR=11 to SR=00, it produces so-called an unknown state, that is, the state is determined based on the delay difference of the feedback lines that cannot be predicted. Check yourself by changing SR from 11 → 00 using LogiScan input control buttons, and then observe the output states and record it in the result section.

Part B: Modify the circuit in Part A to a gated SR-latch as shown below



The input C adds more control on Q and creates a true memory element. The input C becomes a clock input in the Flip-Flop circuits that you will experiment in the next lab. Find the state table using LogiScan, and then record the results in the result section.

Part C: Modify the circuit in Part B to a gated D-latch as shown below



Notice that C is more effectively used in this circuit. Find the state table using LogiScan and then record the results in the result section.

EXPERIMENT #7 RESULTS

Your Name: _____

Witnessed by Instructor or TA: _____

Date _____

Have your TA verify the results after completion of each part.

Part A: State Table for SR-latch

Input		Present State	Next State	
S	R	Q	Q+	Q'+
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Mark the not-allowed cases if you could notice them.

Your observation on change of SR from 11 → 00:

Part B: State Table for gated SR-latch

Inputs and Present States				Next States	
S	R	Q	C	Q+	Q'+
0	0	0	0		
0	0	1	0		
0	1	0	0		
0	1	1	0		
1	0	0	0		
1	0	1	0		
1	1	0	0		
1	1	1	0		
0	0	0	1		
0	0	1	1		
0	1	0	1		
0	1	1	1		
1	0	0	1		
1	0	1	1		
1	1	0	1		
1	1	1	1		

Mark the not-allowed cases and explain why.

Part C: State Table for gated D-latch

Input		Present State	Next State	
C	D	Q	Q+	Q'+
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Mark the not-allowed cases if you found them. Explain why it is different from the S-R latches.