ECE 1315 DIGITAL LOGIC DESIGN

ECE Dept, UMD
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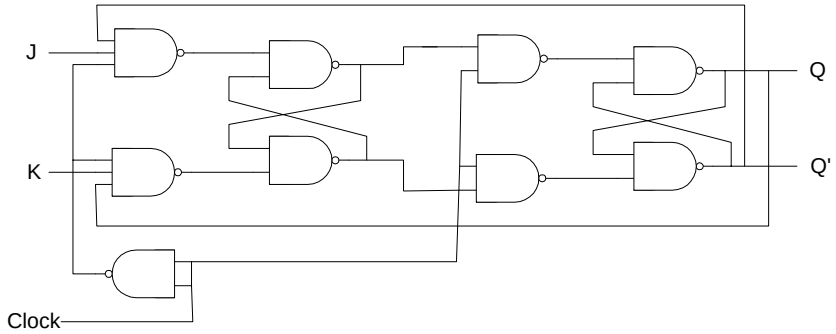
EXPERIMENT # 8: Sequential Circuit: Master-Slave Flip-Flop

In this lab, you will investigate the behavior of a master-slave flip-flop (FF). Master-slave FFs eliminate the direct pass-through conditions of latches by cascading two latches to lock the output signal at the opposite gated signal (clock). That is, if one of the latches is in a gated state (pass through state), the other latch is in a hold state creating a synchronization effect on a clock edge.

Build the JK Master-Slave FF circuit given below on your breadboard. You will need one 74LS10 and two 74LS00's. Make sure that you prepare your own diagram with chip pin numbers in the diagram to minimize the connection errors.

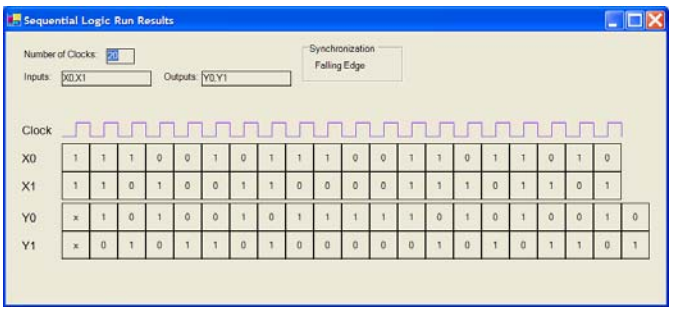


After completing the circuit, please follow the steps provided in Part 1.

Part 1: Test the circuit using LogiScan

1. Connect J and K to the LogiScan X0 and X1. Connect Q and Q' to the LogiScan F0 and F1, respectively. And then connect the Clock input from the LogiScan Pin 22 which is the clock output.
2. Select the check boxes of X0 and X1 for your J and K, and F0 and F1 for your Q and Q'.
3. Next define the input sequences using the "Define New Input Seq." button in the Sequential Logic box of the LogiScan. When you click on the button, you will be asked to enter the number of clock cycles. Enter the number of clock cycles you want to examine. You may enter up to 20 clock cycles.
4. A new window appears for the design of input sequences. Click on the "Randomize Input Sequence" button.
5. If the randomized input sequence does not look random enough, change the values by clicking on the squares.
6. Select the Falling Edge since this FF is a falling edge triggered.
7. Make sure to save the input sequence by clicking the save button. Remember that the run function uses only the saved input sequence.
8. Run the sequential logic by clicking the "Run Defined Input Sequences" button.
9. The run result will appear on a new window.
10. Interpret the timing diagram relation to the tables provided in the Result Section.

You will need to run similar steps in the future for the analysis of all sequential logic circuits. A sample result screen is shown below.



Part 2: Test a JK-FF chip
Get a 74LS76 chip (JK-FF) and connect J, K, Q, and Q' the same way as Step 1. Verify the results with the tables obtained from Part 1. You should see the same sequential behavior as you saw in the circuit built in Part 1.

If your circuit in Part 1 did not work, you should try Part 2: 74LS76 first to learn about the JK-ff behavior. It should help what to expect from the circuit.

EXPERIMENT #8 RESULTS

Your Name: _____

Witnessed by Instructor or TA: _____

Date _____

Record the data observed from Part 1. Assume that time runs vertically in the below table.

J	K	Q	Q'

Deduce the JK-FF state table from the above.

Inputs		Present State	Next States	
J	K	Q	Q+	Q'+
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Since the Part 2 results should be the same as the Part 1, no need to separately record them but show the circuit and results to your TA.