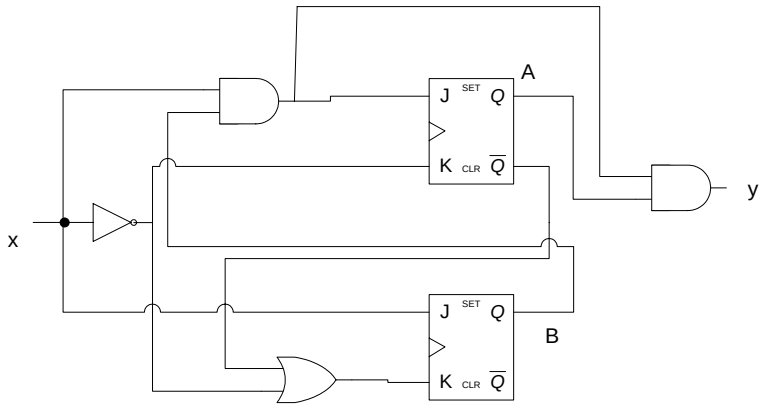
ECE 1315 DIGITAL LOGIC DESIGN

ECE Dept, UMD
April 4, Tuesday, 2006

EXPERIMENT # 9: Analysis of Synchronous Sequential Circuit

The circuit given below has one input x and one output y. Due to the internal sequential states created by FFs, the output not only depends on the current input but also on the history of it. We wish to analyze this behavior and determine its functionality.



This experiment works as follows. First, theoretically analyze the given circuit without actually building it. Next, build the circuit, run it using LogiScan, and verify whether your theoretical analysis matches with the actual run or not. The result section follows these two steps.

For JK-ffs, you can use 74LS76. Please note that Vcc and GND pins are not in the usual positions. Make sure to check the data sheet. Also, make sure to label pin numbers on your circuit diagram to minimize mistakes and to make debugging easier.

EXPERIMENT #9 RESULTS

Your Name: _____

Witnessed by Instructor or TA: _____

Date _____

Show your design process.

Step 1) Derive FF next state and output equations

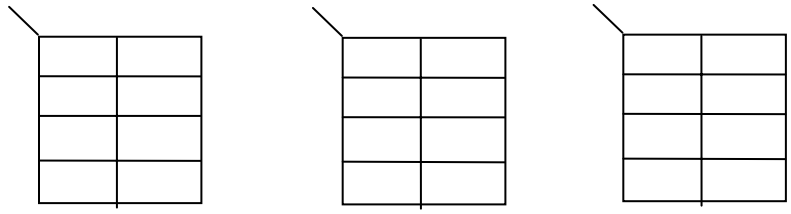
$A(t+1) = J_1Q' + K_1'Q =$_____

$B(t+1) = J_2Q' + K_2'Q =$_____

y = _____

Step 2) Derive the state table

A(t+1) B(t+1) y



State Table Using Binary Bits

PS	NS

State Table Using Letter Symbols

PS	NS

Step 3) Draw the state diagram

Step 4) Create a sample input sequence and find the corresponding output sequence (i.e. the circuit's functionality)

Step 5) Build the circuit by connecting proper inputs, outputs, preset, reset, clock, etc. Record your choices of connections to the LogiScan's inputs and outputs.

Step 6) Generate an input sequence using the LogiScan.
After generating an input sequence by clicking on the "**Define New Input Seq.**" button (you may start with the random sequence and then customize it.), make sure that you save the input sequence by clicking the "Save" button in the "Define New Input Seq." window. Record your input sequence.

Step 7) Run the circuit using LogiScan and compare your circuit run-results with your analytical results (Step 4).
Record your run results and ask an approval from TA.