

Chapter 2: Microcomputer Architecture and Components

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This chapter described the basic architecture of microcomputers and components.

2.1 Computer Architecture

The architectural history of today's computer goes back to the proposal by the following paper: A.W. Burk, H.H. Goldstein, and J. von Neumann, "Preliminary Discussion of the Logical Design of an Electronic Computing Instrument," 1946. This design mainly contributed by von Neumann was originally intended to solve nonlinear differential equations. However, later it has been successfully used in business data processing, information handling, and industrial control as well as in numerical problems. In fact, this design was so well defined that most computers to date -from large computers to microcomputers- are based on it, such that they are called *von Neumann computers*.

The main idea of this design is "A set of instructions called a program is stored in the primary memory, and then the CPU executes the instructions one by one." The overall architecture can be drawn by a simple block diagram as shown in Figure 2.1.

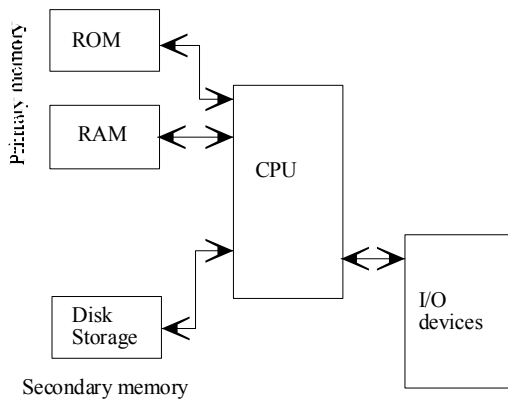


Figure 2.1: von Neuman architecture

generally used as the system or monitor programs to process the power on reset in computers.

2.2 Microcomputer

Due to technological advances in ICs, it is now possible to put a controller (also called a sequencer circuit) and data operator in a single LSI or VLSI chip. Such a combination of data operator and controller is called a **microprocessor**. If a memory, input/output (I/O) modules, and a clock circuit are added to a microprocessor, the result is called a **microcomputer**.

2.3 Microcomputer Components

2.3.1 ROM (Read Only Memory)

ROMs are the memory devices that retain its data even if the power is disconnected. It is

Mask-programmable ROM (or mask ROM)

ROMs are programmed by the pattern of connections and no connections in one of the masks used in the IC manufacturing process. To program or write information in to the ROM, the customer gives the manufacturer a listing of the ROM contents, using a floppy disk or other medium. The manufacturer uses this information to create one or more customized masks to manufacture ROMs with the required pattern.

ROM manufacturers usually impose a mask charge of several thousands dollars for the customized aspects of mask ROM production. Because of mask charges and the four-week delay typically required to obtain programmed chips,

mask ROMs are normally used today only in high-volume applications. For low-volume applications, there are more cost effective choices.

Programmable Read Only Memory (PROM)

It is a one-time writeable by a PROM programmer. A PROM is manufactured with all of its diodes or transistors connected. This corresponds to having all bits at a particular value, typically 1. The PROM programmer can be used to set desired bits to opposite value (typically 0), by vaporizing tiny fusible links inside the PROM corresponding to each bit. A link is vaporized by selecting it using the PROM's address and data lines, and then applying a high-voltage pulse (10 to 30V) to the device through a special input pin.

Erasable PROM (EPROM)

It is programmed like a PROM, but it can also be erased to the all-1's state by exposing it to ultraviolet light. Each transistor has two gates, floating and non-floating. The floating gate is unconnected and is surrounded by extremely high-impedance insulating material. To program an EPROM, the programmer applies a high voltage to the non-floating gate at each bit location where a '0' is to be stored. This causes a breakdown in the insulating material and allows a negative charge to accumulate on the floating gate. When the high voltage is removed, the negative charge remains. During the subsequent read operation, the negative charge prevents the MOS transistor from turning on when it is selected. The insulating material surrounding the floating gate becomes slightly conductive if it is exposed to ultra violet light with a certain wave length. Thus. EPROMs can be erased by exposing the chips to ultraviolet light, typically for 5-20 minutes.

Electrically Erasable PROM (EEPROM)

It is similar to EPROM except that individual stored bits may be erased electrically. The floating gates in an EEPROM are surrounded by a much thinner insulating layer, and can be erased by applying a voltage of the opposite polarity as the charging voltage to the non-floating gate.

2.3.2 RAM (Random Access Memory)

Data can be read or written to RAM without any special voltages or light source. A data word in the memory is typically read or written one word at a time after selecting the address of it. However, the data stored in RAM is lost if the power to the IC chip is disconnected.

Static RAM (SRAM)

The information remains stored as long as power is applied to the chip, unless the same location is written again.

Dynamic RAM (DRAM)

The data stored at each location must be periodically refreshed by reading it and the writing it back again, or else it disappears.

DRAM is by far the cheapest to build. Newer and faster DRAM types are developed continuously.

Currently, there are at least four types:

- FPM (Fast Page Mode)
- ECC (Error Correcting Code)
- EDO (Extended Data Output)
- SDRAM (Synchronous Dynamic RAM)

A brief explanation of DRAM types

FPM was the traditional RAM for PCs, before the EDO was introduced. It is mounted in SIMM modules of 2, 4, 8, 16, or 32 MB. Typically, it is found in 60 ns or 70 ns versions. 60 ns is the fastest and the one to use. You cannot mix different speeds on the same Pentium motherboard.

EDO is an improvement of FPM RAM. EDO stands for “Extended Data Out” which means the chip asserts the data on its output pins longer (probably under special hardware handshaking), even while the next requested address is strobed into the address lines. It makes memory access faster because you can do the addressing and reading concurrently. By switching from FPM to EDO, one can expect a performance improvement of 2 to 5 percent. EDO RAM are usually sold in 60 ns versions. A 50 ns version is available at higher cost.

ECC RAM is a special error correcting RAM type. It is especially used in servers.

Synchronous DRAM (SDRAM) is a generic name for various kinds of DRAM that are synchronized with the clock speed that the microprocessor is optimized for. This tends to increase the number of instructions that the processor can perform in a given time. The speed of SDRAM is rated in MHz rather than in nanoseconds (ns). This makes it easier to compare the bus speed and the RAM chip speed. You can convert the RAM clock speed to nanoseconds by dividing the chip speed into 1 billion ns (which is one second). For example, an 83 MHz RAM would be equivalent to 12 ns. It comes only in 64 bit modules (long 168 pin DIMMs).

RAMBUS Dynamic Random Access Memory (RDRAM) is a future RAM type. Intel and others have great expectations from this type. RDRAM promises to transfer up to 1.6 billion bytes per second. The subsystem consists of the RAM, the RAM controller, and the bus (path) connecting RAM to the microprocessor and devices in the computer that use it. Direct Rambus (DRDRAM), a technology developed and licensed by the Rambus Corporation, will be used with Intel microprocessors beginning in 1999. High-speed RAM is expected to accelerate the growth of visually intensive interfaces such as 3-D, interactive games, and streaming multimedia. Rambus is intended to replace the current main memory technology of dynamic random access memory (DRAM). Much faster data transfer rates from attached devices such as videocams using Firewire and the Accelerated Graphics Port (AGP) make it important to reduce the bottleneck in getting data into the computer, staging it in RAM, and moving it through the microprocessor and to the display or other output devices.