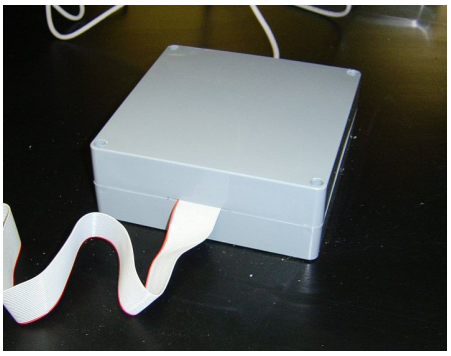
Department of Electrical and Computer Engineering
ECE1315: Digital System Design
LogiScan User Manual

What is LogiScan?



The LogiScan is a USB-based digital-circuit testing system developed by Prof. Taek Kwon as a testing tool for the digital circuits used in the ECE 1315 Lab. It consists of an interface box and software that runs on a PC. The interface box is controlled from a PC through a USB connection and generates input patterns for digital-logic circuits. The outputs of the circuit connected to the LogiScan interface box is scanned in real-time and displayed on the PC screen. LogiScan is capable for testing both combinatorial and synchronous sequential circuits.

Pin-out diagram of the 24 pin in-line Connector

The most important information that students need to know before using the LogiScan is the pin-outs of the 24-pin ribbon-cable connector of the interface box. This connector shown in Figure 1 provides all necessary interfaces between your breadboard and the LogiScan. Please note where the pin #1 is in relation to the side of ribbon cable. Figure 1 is the top view of the connector, and pin #1 is located left top of the connector.

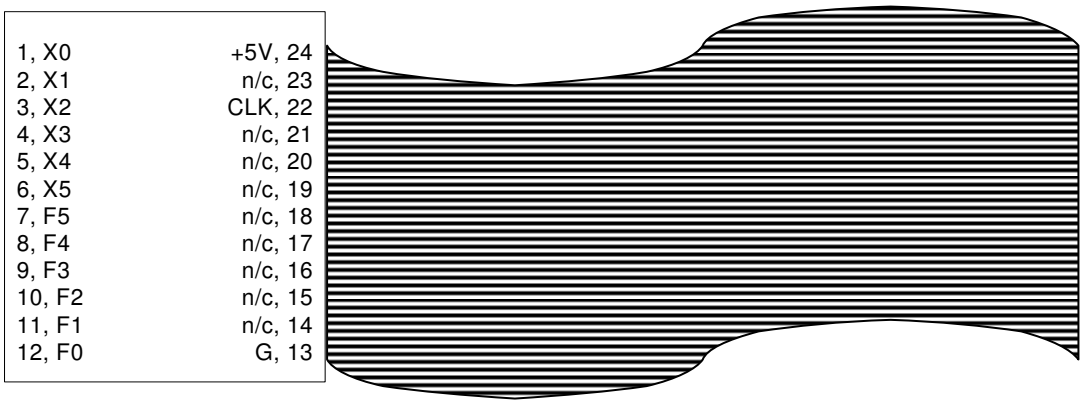


Figure 1: Pin-outs of 24pin inline connector

Pins 1,2,…,6: X0, X1, ..., X5
LogiScan generates logic signals and then sends them out to these pins so these pins must be connected to the inputs of your circuit. The bit patterns consisting of logic-0 and logic-1 (0 or 5Volts) can be controlled toggling the red squares or through an input table.

Pins 12,11,…,7: F0, F1, ..., F5
These pins must be connected to the outputs of your circuit. The LogiScan reads these pins and displays the results on the PC screen. Note that pin numbers are in a reverse order in relation to F0,..,F5.

Pin 24: +5V
This pin provides +5V power source and should be connected to Vcc of your circuit. Every TTL chips require +5V and 0V power connection, and this pin should be used for connecting the +5V supply of the chip.

Pin 13: G
This pin provides 0V, i.e., GND and should be used to connect the GND pin of your chip.

Pin 22: CLK
This pin provides a clock signal for running sequential logic circuits.

Controlling signals using the LogiScan software

The software is run by double clicking the icon 

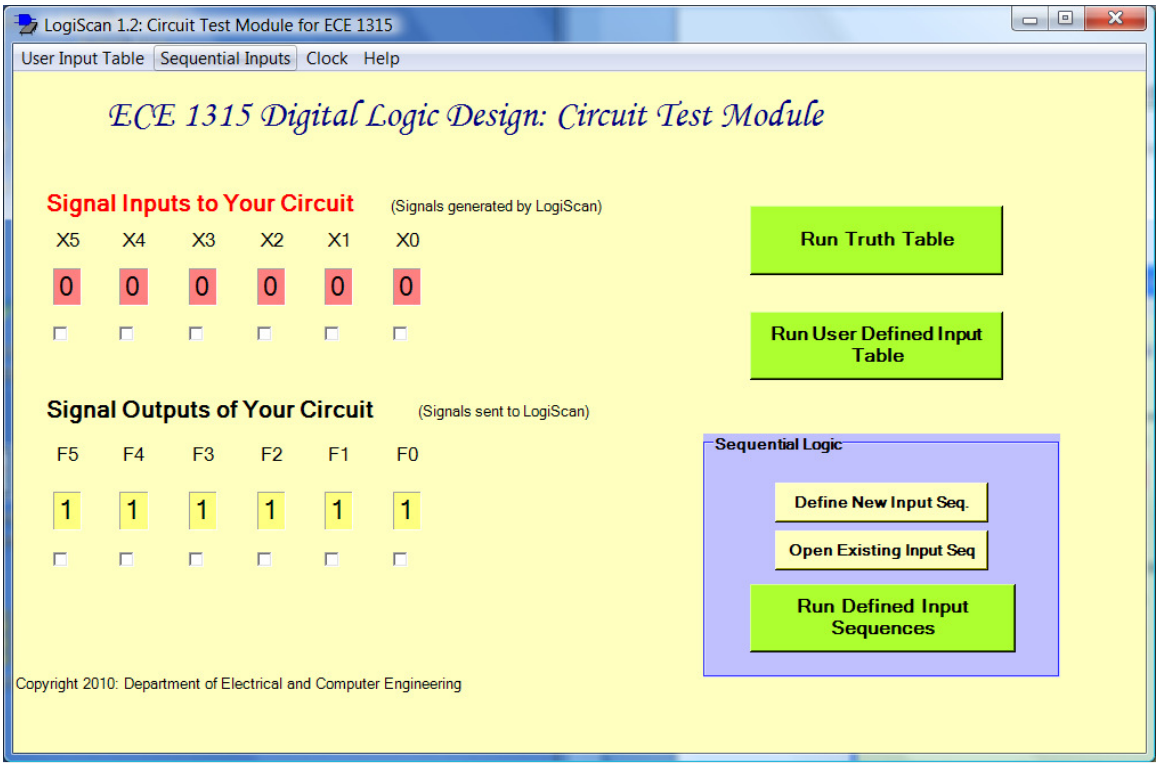


Figure 2: LogiScan screen

LogiScan produces +5V for logic-1 and 0V for logic-0 and sends out the signals to the pins X0 through X5. **The red squares under the labels X0-X5 toggle between 0 and 1 when you click on it using the left mouse button**, which then immediately sends the corresponding voltages (0V or +5V) to the corresponding pins. **The check boxes under the red squares are used to define used (or connected) inputs.**

The outputs of your circuit are read when you connect them to pins F0-F5. The logic-1 or 0 value in the yellow boxes under the label "**Signal Outputs of Your Circuit**" is the real-time read-out results corresponding to +5V or 0V on the respective pin. The check boxes under the yellow boxes are used to define which outputs are used for generating the truth table.

Combinational Logic: A Walk-Through Example

This example illustrates how to connect and test an OR function using a 74LS32 chip. A 74x32 chip includes four 2-input OR gates, and we will use only one of the four gates. Using your breadboard, connect the two inputs of the first OR gate to X0 and X1 and the output of the OR gate to F0, and also Vcc to +5V and GND to G, as shown in the connection diagram in Figure 3.

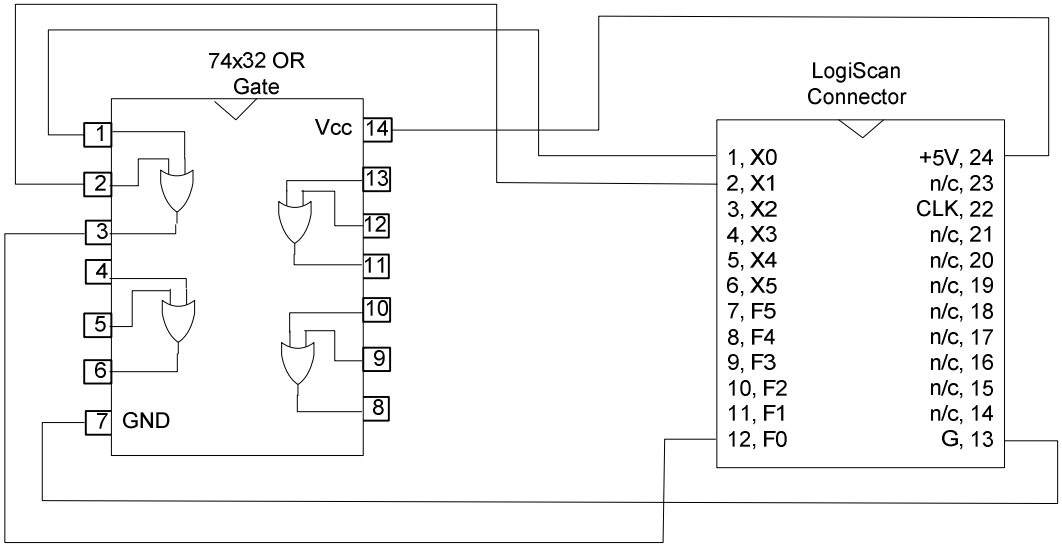


Figure 3: Connection diagram of an OR gate test circuit

Next, using the LogiScan software toggle the signals of X0 and X1 by clicking on the red squares and observe the output, F0. You should be able to observe the following OR relation.

X1	X0	F0
0	0	0
0	1	1
1	0	1
1	1	1

Now, select the check boxes under X0, X1, and F0, and then click the "**Run Truth Table"** button. You should be able to see a pop-up window that contains the circuit's truth table, i.e. Figure 4.

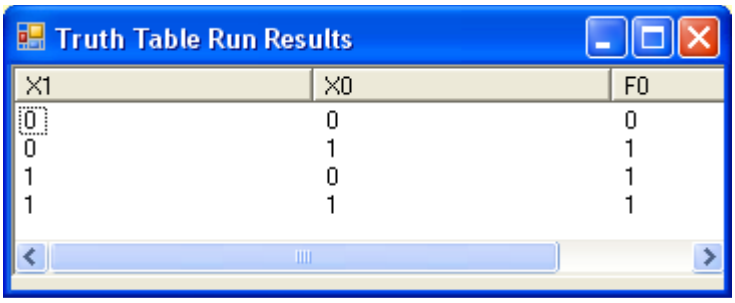


Figure 4: Truth table for OR

Partial input combination tests

When a combinational circuit has many inputs, often only a part of input combinations needs to be tested. In such a case, you need to build your own input test patterns. To define the input patterns, select the menu item: "**User Input Table" → "Build New One"**. For illustration, above OR gate connection is used. Suppose that you only wish to test three input patterns then "3" is entered in the "**Input Table"** dialog (Figure 5), which brings out the "**User Defined Input Table"** window (Figure 6).

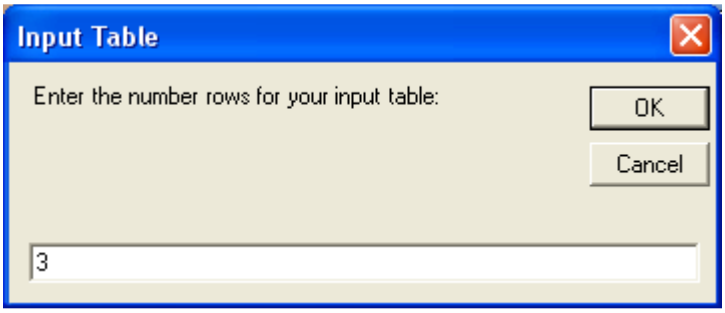


Figure 5: Number of entries in the Input Table dialog

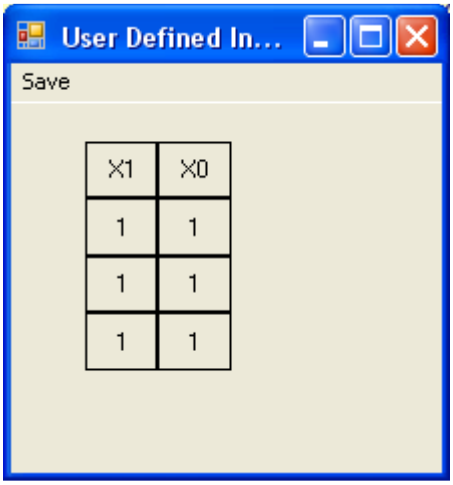


Figure 6: User defined input table. You can design input patterns by toggling the input bits.

The default values the **User Defined Input Table** are all logic-1's and the desired input patterns are generated by clicking on the value which toggles between 0 and 1. Various

input patterns can be easily created by toggling the input bits. For this example, the input patterns are created as shown Figure 7.

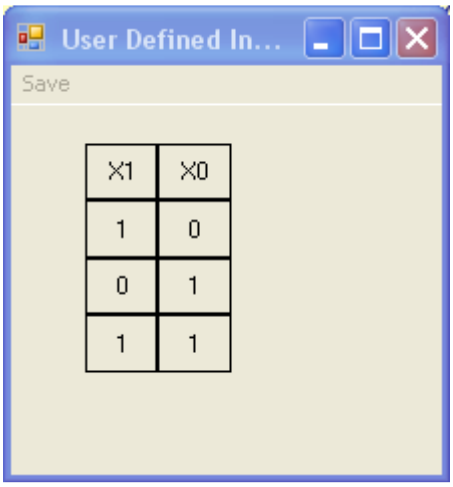


Figure 7: User generated input patterns

After creating the table, make sure to save the input patterns by clicking **Save/Save Table and Exit**. It is important to save the inputs defined since the truth table is run based on the saved patterns. And then run the circuit using the "**Run User Defined Input Table**" button. The final output of the example is shown below (Figure 8).

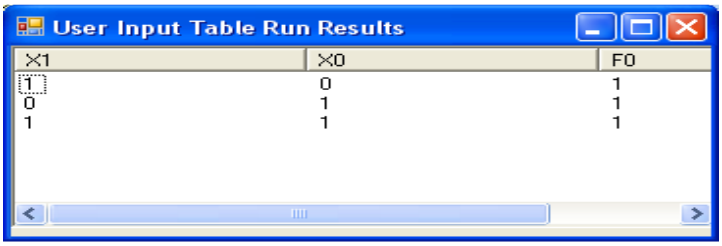


Figure 8: Truth table output

Synchronous Sequential Logic

In a sequential circuit, the output is no longer just a function of the present input signals but also a function of past history of inputs. More specifically, the circuit may produce a different output even if the present inputs are the same but if the past inputs were different. It also uses a clock to differentiate the timing of signals on the past and the present.

Testing a sequential logic circuit requires the following steps.

- Connect your circuit to LogiScan, i.e., inputs of your circuit to X0-X5 and outputs of your circuit to F0-F5.
- Connect the clock input of your circuit to the LogiScan Clock pin (pin 22)
- Select the check boxes for the inputs and outputs you connected.
- Next define the input sequences using the "**Define New Input Seq.**" button in the Sequential Logic box (purple box).
- Make sure to save the input sequence by clicking on the **Save** button. Remember that the run function uses only the saved input sequences. If saving is done, you can now close the **Input Sequence** window.
- Run your circuit by clicking on the "**Run Defined Input Sequences**" button.
- The run result will appear on a new window and you should analyze the results to check if the output sequences are correct. If it is not, you will need to correct your circuit.

Walk-Through Example: D-FF

Let's test the functionality of a D-FF Q* output (* denotes NOT). 74x74 has two D-FFs, and we will use only one of them. The output sequence expected is the inverted input sequence with one clock cycle delay.

Step 1) First, make connections on your breadboard as show in Figure 9. Notice that input D is connected to X0, the output Q* is connected to F0, and CLK to clock. CLR* and PRE* are connected to +5V (Logic 1 or Vcc).

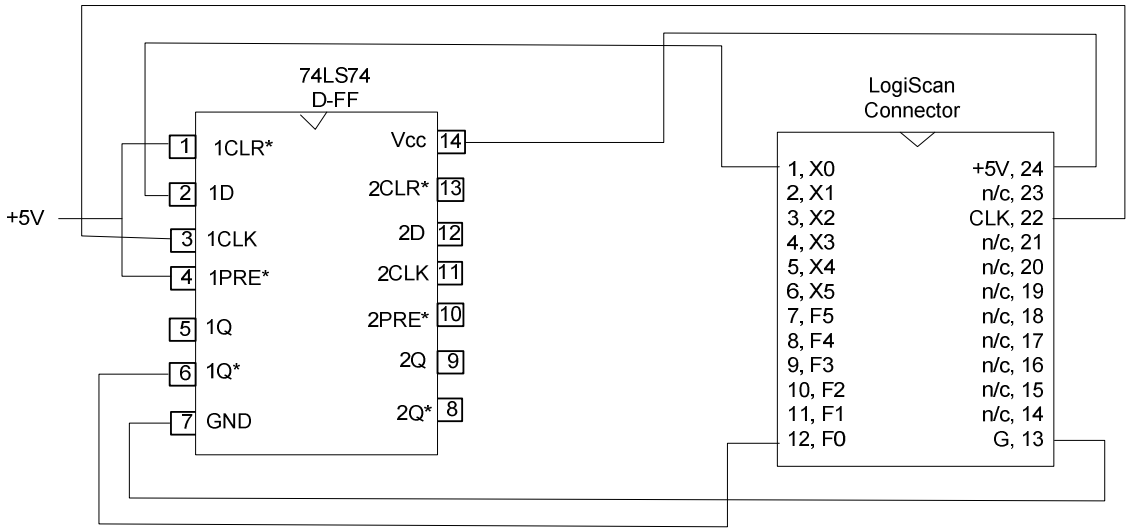
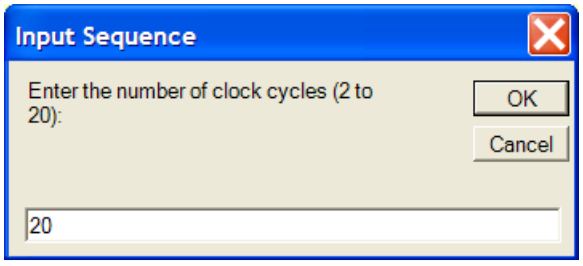


Figure 9: D-FF test circuit

Step 2) Since X0 is used as input sequence and F0 is used as the output sequence, place check marks on both X0 and F0.

Step 3) Define the input sequence.
Click on the "**Define New Input Seq**" which would bring up the following screen. Enter 20 and click OK.



Next, you will see the input sequence screen. Choose the Rising edge radio button since 74LS74 is synchronized to the rising edge of the clock and then randomize the input sequence by clicking on the "**Randomize Input Sequence**" button for this particular example. You can click on the individual input sequence to design your own sequence.

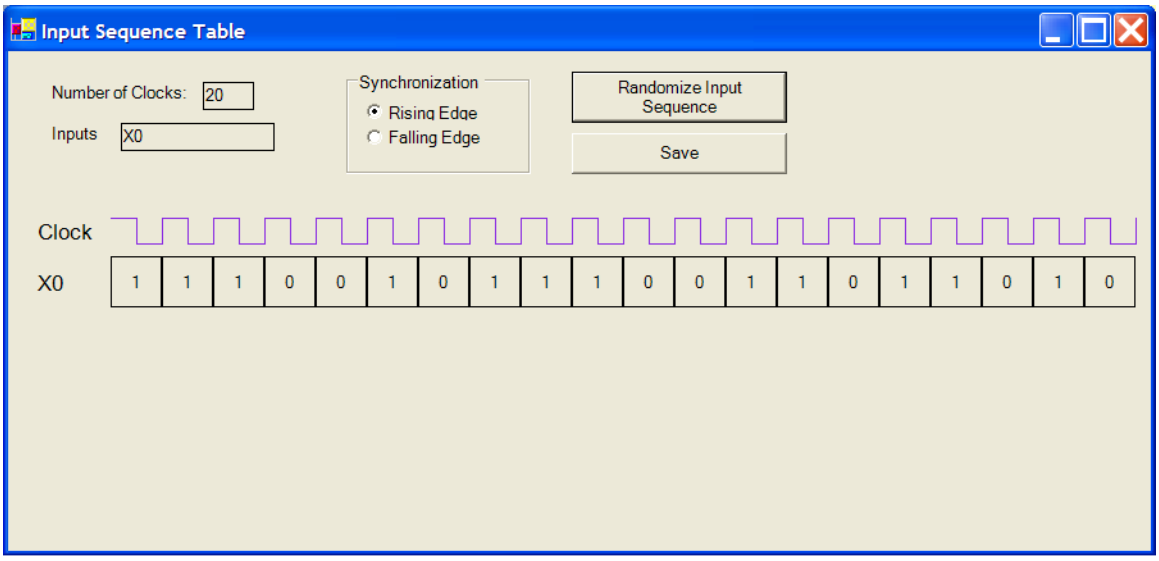


Figure 10: Input sequence edit

Next, the important step is to save the generated sequence using the **Save** button. Click on the **Save** button and close the Input Sequence Table. Please remember that the saved sequence is the one that the LogiScan uses.

Step 4) Run the sequential circuit by clicking on the "**Run Defined Input Sequences**" button.

Step 5) Analyze the run results, i.e. the output sequence
The screen capture of the run result is shown in Figure 11. Notice that all input values appear in the output as inverted values after each rising edge of the clock, i.e., one clock delay. This is exactly what Q* of a D-FF supposed to function.

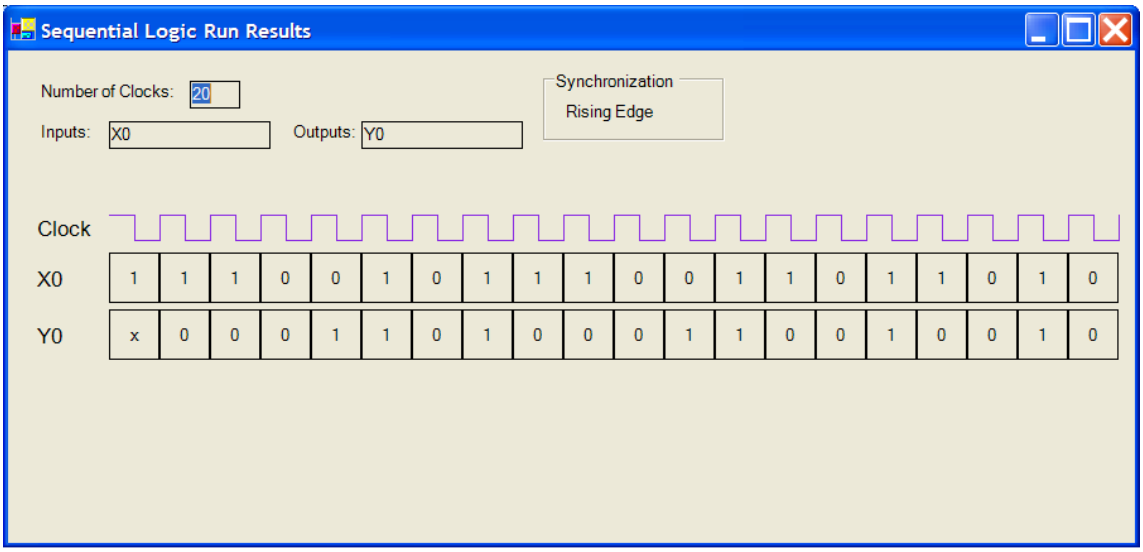


Figure 11: Finial run output of the D-ff circuit

You have now successfully completed this walk-through example.

Remarks

In summary, LogiScan provides six programmable input signals and six ports for output display. Any combinational and synchronous sequential logic circuits having less than six inputs and outputs can be tested by using the steps shown in the above walk-through examples. It is essentially a logic analyzer simplified for small circuits.

One of the important things to remember is to save the input sequence or patterns after you created them. LogiScan only uses the saved input patterns or sequences to capture the outputs of the test circuit. Once it is saved, the data is in the memory and you can review the data by clicking on the menu "**Sequential Inputs/Open Existing**" for the sequence input and the menu item "**User Input Table/Open Existing**" for the combinational logic.

LogiScan was developed by Prof. Taek Kwon at the ECE Department. If you experience any problems, please first talk to your TA or instructor. If the issue is still not resolved, please contact Prof. Kwon.