**ECE 1315: Digital System Design**

*ECE Required Course - Spring 2006*

**2003-2005 Catalog Course Description:**
Binary number system and digital coding techniques. Boolean algebra, combinational logic circuits, and minimization techniques. Synchronous sequential circuits and state reduction techniques. Medium Scale Integration (MSI) combinational components

**Prerequisites:**
None

**Course Outcomes: (Students should …)**

- Understand the basic logic operations and their use in the implementation of logic functions (a)
- Experience the use of logic gates, and the use of manuals and data sheets to get the necessary information (b, k, n)
- Learning the basic characteristics of timing, power, fan-out, delay, etc., involved in the implementation of logic systems (a)
- Understand the basic differences between combinational and sequential logic networks (a, l, n)

**Educational Goals:**
This is a first course in digital/computer system design from which students learn the basic design principles of combinational and sequential logic circuits. In this course, students learn number systems and their conversions, Boolean algebra, families of logic gates, circuit minimization techniques, and analysis and synthesis of combinational and sequential logic circuits. More complex implementations using combinations of both types of circuits and functional logic units such as decoders, multiplexers, counters, adders, etc are also learned. Students learn implementation aspects of digital circuits through laboratory experiments designed base on TTL family of chips.

Laboratory projects:
- Familiarization with the TTL family of gates (AND, NAND, OR, NOR and NOT operations).
- Basic combinational circuits and function minimization.
- NAND-NAND and NOR-NOR networks.
- Iterative networks
- Data selectors and decoders
- Transparent latches and Flip-Flops
- Synchronous sequential circuits
- Counters
- 7-segment display applications

**Relationship to ECE Program Objectives:**

- Introduces students to the basic techniques of designing, debugging and implementing a system (a, c, e, k)
- Gives students the experience to apply theoretical knowledge in solving practical problems (a, e)
- Exposes students to the use of lab equipment, and input-output data generation and interpretation (b, n)
- Prepares students for advanced courses in digital systems, microcomputer design and applications (a, b, n)
ECE 1315: Syllabus – Spring 2006

Professor:  Dr. Taek Kwon  Office: MWAH 253  Phone: 726-8211
Office Hours: M,W 11:00-12:00 and whenever my door is open
Email:  tkwon@d.umn.edu  Web Page: http://www.d.umn.edu/~tkwon

Course Web Site: http://www.d.umn.edu/~tkwon/course/1315/1315.html

Lecture Place & Time:  BohH 112; MWF 10:00-10:50am
Lab Place & Time:  MWAH 393; Tuesday 9:00am-12:00pm (Sec 2), 1:00am-4:00pm (Sec 3)


Assessment:  Exam-1: 15%, Exam-2: 25%, Final Exam: 35%, Labs & Reports: 20%, HW:5 %

<table>
<thead>
<tr>
<th>DATES</th>
<th>TOPICS</th>
<th>Textbook, Lab</th>
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<tbody>
<tr>
<td>1/18-20</td>
<td>Introduction to digital Systems. Number Systems</td>
<td>Chap.2, No Lab</td>
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<tr>
<td>1/23-27</td>
<td>Operations in binary and hexadecimal. Boolean algebra.</td>
<td>Chap.2, 3, LAB #1</td>
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<td>1/30-2/3</td>
<td>Boolean theorems and properties. Basic gates &amp; simple circuits</td>
<td>Chap 3, LAB #2</td>
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<td>2/6-10</td>
<td>Min/Max term, K-map</td>
<td>Chap 3, LAB #3</td>
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<td>2/13-2/17</td>
<td>Advanced K-map and Quine McCluskey method</td>
<td>Chap 4, LAB #4</td>
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<td>2/20-2/24</td>
<td>More Quine McCluskey methods, <strong>Exam 1 (2/24)</strong></td>
<td>Chap 4, LAB #5</td>
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<td>2/27-3/3</td>
<td>Adders, mux, and decoders</td>
<td>Chap 5, LAB #6</td>
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<td>3/6-3/10</td>
<td>PAL, PLA, ROM</td>
<td>Chap 5</td>
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<td>3/20-3/24</td>
<td>Latches, flip flops</td>
<td>Chap 6, LAB #7</td>
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<td>3/27-31</td>
<td>Analysis of synchronous sequential logic circuits.</td>
<td>Chap 7, LAB #8</td>
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<td>4/3-7</td>
<td>Counter design, registers, shift registers,</td>
<td>Chap 6, LAB #9</td>
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<td>4/10-14</td>
<td>Design using counter modules,</td>
<td>Chap 6, LAB #10</td>
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<tr>
<td>4/17-21</td>
<td>Design of sequential network, <strong>Exam 2 (4/21)</strong></td>
<td>Chap 7, LAB #11</td>
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<td>4/24-28</td>
<td>Partition and implication table</td>
<td>Chap 7, LAB #12</td>
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<td>5/1-5</td>
<td>Simplification of sequential circuits, cont.</td>
<td>Chap 7</td>
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<td>5/11</td>
<td>FINAL EXAM: Thursday May 11, 8:00-9:55am</td>
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Accreditation Outcomes addressed by this class: (Students should demonstrate …)
(a) An ability to apply knowledge of mathematics, science and engineering
(b) An ability to design and conduct experiments, as well as to analyze and interpret data
(c) An ability to design a system, component, or process to meet desired needs
(e) An ability to identify, formulate, and solve engineering problems
(k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice
(l) A knowledge of computer software and hardware as demonstrated by the Computer Science Minor embedded in the program
(n) An ability to work in a hands-on laboratory in most of the required courses

Individuals who have any disability, either permanent or temporary, which might affect their ability to perform in this class, are encouraged to inform the instructor at the start of the semester. Adaptations may be made as required to provide for equitable participation.

Prepared by  Taek Kwon  1/14/2006
Name  date