EE 5315 - Multiprocessor-Based System Design
Technical Elective in Digital Systems Category - Fall 2014

2014-2015 Catalog Course Description:
Parallelism, interconnection networks, shared memory architecture, principles of scalable performance, vector computers, multiprocessors, dataflow architecture, and supercomputers. (3hrs lecture)

Prerequisites:
(3 cr; QP-3325, CS 5520; SP 4305; CS 5631; A-F only)

Course Outcomes (Students should …):
- Understand performance metrics and be able to analyze scalability and speedup factors of multiprocessor systems (a, b, c, j)
- Learn various parallel computer models and be able to design them in a block diagram level (e, j, k)
- Understand thread models, synchronization, mutual exclusion, critical regions, and semaphore (c, k, l)
- Understand various distributed memory models and the latency tolerance issues (a, c, k)
- Understand distributed cache models and cache coherence protocols (a, c)
- Learn examples of shared memory models and symmetric multiprocessors (c, e, j)
- Know the architectures of commercial super computers (j)
- Learn how clustering of computers works and can increase the availability (c, e, j)
- Learn linear/nonlinear pipeline design techniques and be able to apply them into application design (a, b, c, e, k)
- Complete the assigned simulation project using multithreads (parallel programming (e, g, l, n)

(a through n” are student outcomes)

Educational Goals:
This senior or entry level graduate course is designed to expose students to advanced design techniques in high-performance computers. It provides a foundation for understanding the design principles incorporated in modern computers that use multiple processors or cores. The course covers computer system performance metrics and measures, scalability, parallel architectures, cache coherence, consistency, latency hiding, and synchronization.

The course will briefly review the basics of advanced single processor architectures, since they serve as the building blocks of multiprocessor systems. In particular, linear and nonlinear pipelined design techniques will be reviewed. It then focuses on learning the design techniques of shared memory systems and the corresponding symmetric multiprocessors. Next, distributed memory based scalable systems that employ thousands of processor is studied along with various scalability issues.

Several projects will be given to model the behavior or simulate hardware interactions.

Relationship to EE Program Objectives:
- This course is one of the EE technical elective courses that provides senior level students to an opportunity to explore advanced topics within the digital systems specialty.
- Extends fundamentals of computer hardware design to an advanced level
- Exposes students to performance measurement metrics that help understand the true performance of multiprocessor computing systems
EE 5315 – Syllabus – Fall 2014 (draft)

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Office Hours: MWF 5:15-6:00pm, web: www.d.umn.edu/~tkwon

Lecture: Room & Time: MWAH 191, 4:00-5:15pm MW

Textbook: David Culler and Jaswinder Signh, Parallel Computer Architecture, Morgan Kaufmann Inc., 1999


Computer Usage: Students must complete a course project that requires multithreading, and critical region synchronization and communication.

Assessment: Projects+ HW: 25%, Midterm: 35%, Final: 40%

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<tr>
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<td>12/15</td>
<td>Final Exam, 8:00-9:55am</td>
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Note: The detailed topics and dates may be adjusted during the semester depending on the class progress.

Outcomes addressed by this course:
(a) An ability to apply knowledge of mathematics, science, and engineering
(b) An ability to design and conduct experiments, as well as to analyze and interpret data
(c) An ability to design a system, components, or process to meet desired needs
(e) An ability to identify, formulate, and solve engineering problems
(g) An ability to communicate effectively in writing and orally
(j) A knowledge of contemporary issues
(k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice
(l) A knowledge of computer software and hardware as demonstrated by the Computer Science Minor embedded in the program
(n) An ability to work in a hands-on laboratory in most of the required courses

Students with disabilities: It is the policy and practice of the University of Minnesota Duluth to create inclusive learning environments for all students, including students with disabilities. If there are aspects of this course that result in barriers to your inclusion or your ability to meet course requirements – such as time limited exams, inaccessible web content, or the use of non-captioned videos – please notify the instructor as soon as possible. You are also encouraged to contact the Office of Disability Resources to discuss and arrange reasonable accommodations. Please call 218-726-6130 or visit the DR website at www.d.umn.edu/access for more information.

Prepared by Dr. Taek M. Kwon