

Special Issue on Analog and Mixed-Signal Design Automation

Call for Papers

Design of analog and mixed-signal circuits and systems is a major challenge in today's system-on-chip (SoC). The reason is twofold. First, with the migration of device technology to the nanoscale domain (sub-90nm), device scaling effects, reduced supply voltage, and increasing design density present serious challenges to the designers. Second is the reduced time-to-market window. There is constant pressure on the designers to produce high-performance designs in the first attempt. To cope with the situation, designers need innovative design methodologies and associated design automation tools. Design of analog systems is typically categorized into three levels: high level, circuit level, and layout level. However, each level can be further refined depending on the desired granularity. High-level design of analog systems includes design tasks such as architecture generation, specification translation, performance modeling, and design verification. Circuit-level design takes on topology selection and transistor sizing. Layout-level design involves layout generation and postlayout verification.

The main focus of this special issue will be on the recent advances in methodologies, algorithms, and tools for design automation of analog and mixed-signal systems. Potential topics include, but are not limited to:

- Hierarchical top-down, bottom-up, or integrated design methodology
- Architecture/topology generation or invention
- Specification translation
- Design verification
- Performance modeling
- Automated circuit sizing
- Automated circuit layout
- Computer-aided signal integrity analysis and design
- Statistical analysis and yield-aware or thermal-aware statistical design
- Intellectual property characterization, design reuse, and automated technology migration
- Automated testing

Before submission authors should carefully read over the journal's Author Guidelines, which are located at <http://www.hindawi.com/journals/jece/guidelines/>. Prospective authors should submit an electronic copy of their complete manuscript through the journal Manuscript Tracking System at <http://mts.hindawi.com/> according to the following timetable:

Manuscript Due	Friday, 6 April 2012
First Round of Reviews	Friday, 29 June 2012
Publication Date	Friday, 24 August 2012

Lead Guest Editor

Hua Tang, Department of Electrical and Computer Engineering, University of Minnesota Duluth, Duluth, MN 55811, USA; htang@d.umn.edu

Guest Editors

Soumya Pandit, Institute of Radio Physics and Electronics, University of Calcutta, West Bengal, Kolkata 700009, India; soumya_pandit@ieee.org

Mark Po-Hung Lin, Department of Electrical Engineering, National Chung Cheng University, Minhsiung, Chiayi 62102, Taiwan; marklin@ccu.edu.tw