Basic OpAmp Design and Compensation

Chapter 6

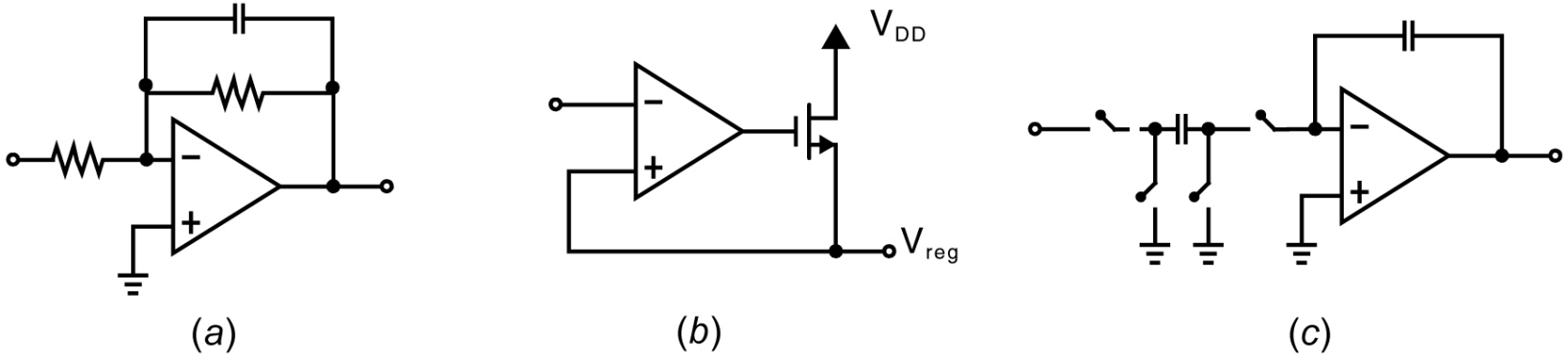
6.1 OpAmp applications

Typical applications of OpAmps in analog integrated circuits:

(a) Amplification and filtering

(b) Biasing and regulation

(c) Switched-capacitor circuits



Chapter 6 Figure 01

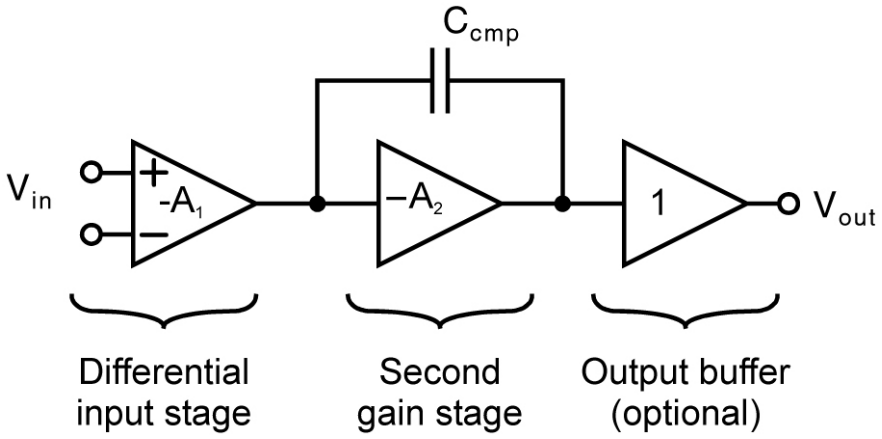
The classic Two-State OpAmp

The two-stage circuit architecture has historically been the most popular approach to OpAmp design.

It can provide high gain and high output swing.

It is an excellent example to illustrate many important design concepts that area also directly applicable to other designs.

The two-stage refers to the number of gain stages in the OpAmp. The output buffer is normally present only when resistive loads needs to be driver. If the load is purely capacitive, it is not needed.



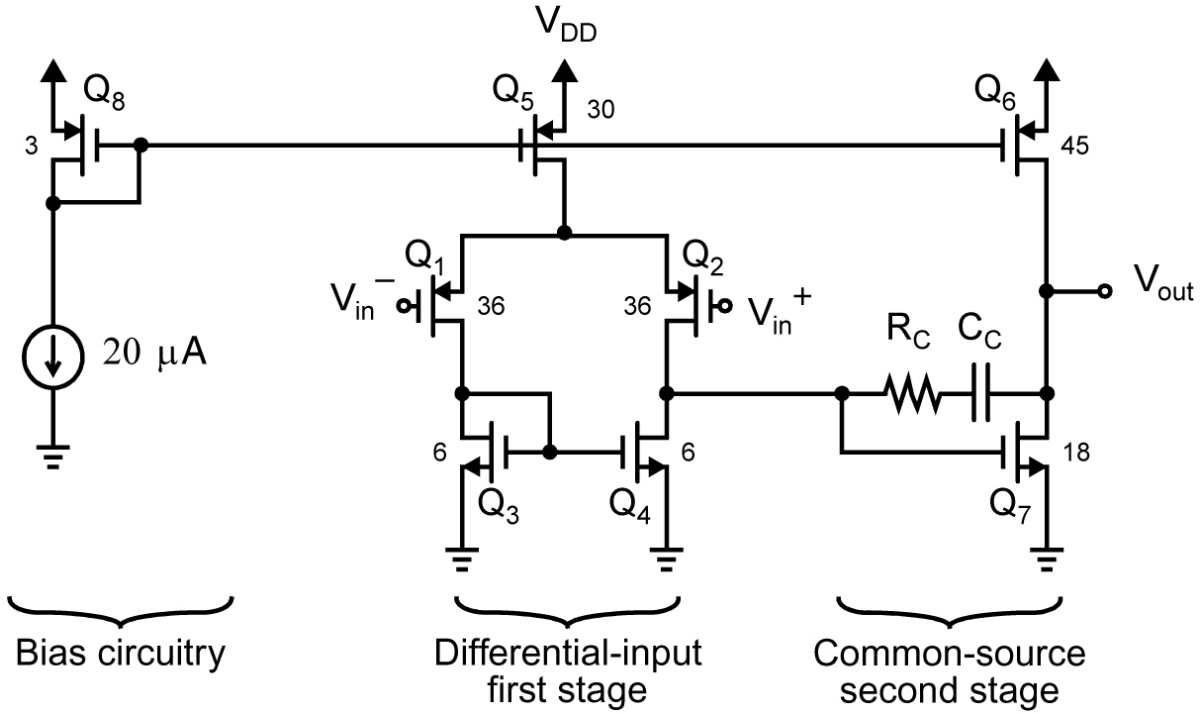
Chapter 6 Figure 02

The classic Two-State OpAmp

The load is assumed capacitive.

The first stage is a pMOS differential pair with nMOS current mirrors. Second stage is a common-source amplifier.

Shown in the diagram are reasonable widths in 0.18um technology (length all made 0.3um). Reasonable sizes for the lengths are usually 1.5 to 10 times of the minimum length (while digital circuits usually use the minimum).



Chapter 6 Figure 03

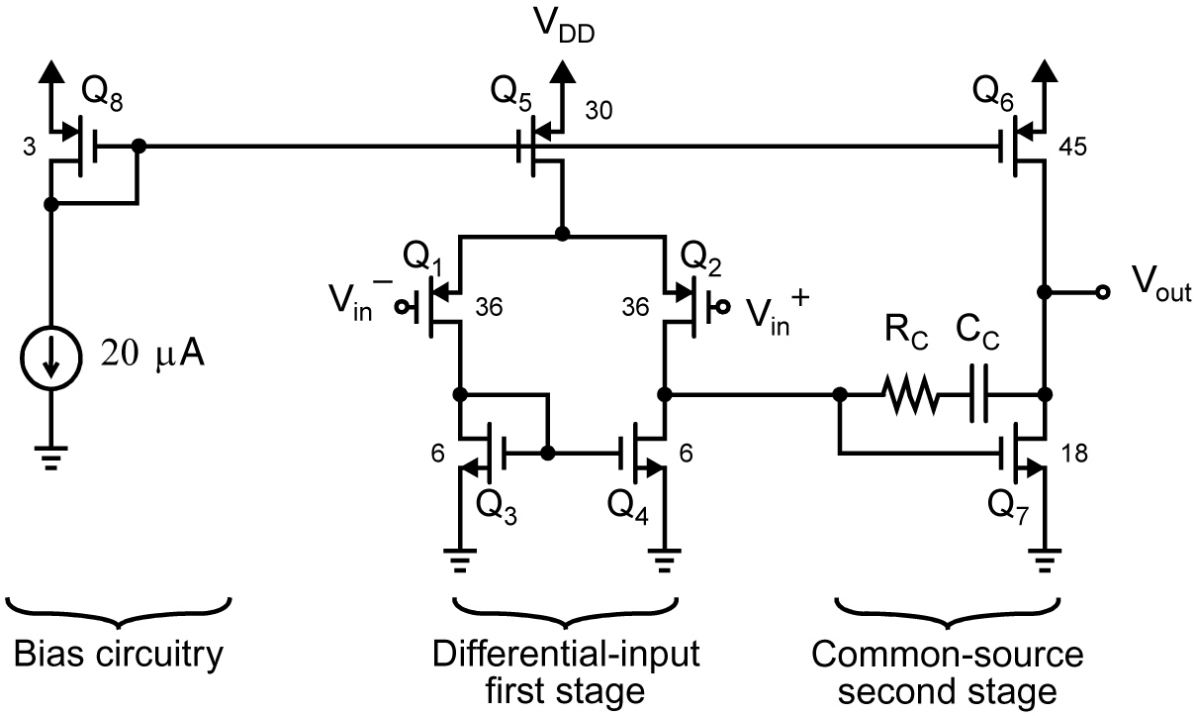
6.1.1 OpAmp gain

For low-frequency applications, the gain is one of the most critical parameters. Note that compensation capacitor Cc can be treated open at low frequency.

gain of the first stage $A_{v1} = -g_{m1}(r_{ds2} \| dr_{ds4})$ $g_{m1} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 \frac{I_{bias}}{2}}$

The second gain stage is simply a common-source gain stage with a p-channel active load, Q_6. Its gain is given by

$$A_{v2} = -g_{m7}(r_{ds6} \| r_{ds7}) \quad (6.3)$$



Chapter 6 Figure 03

Overall gain $A_v = A_{v1} * A_{v2}$

Example 6.1 (page 244)

Find the gain of the opamp shown in Fig. 6.3. Assume the power supply is $V_{DD} = 1.8$ V and a purely capacitive load. Assume the process parameters for the 0.18-µm process in Table 1.5.

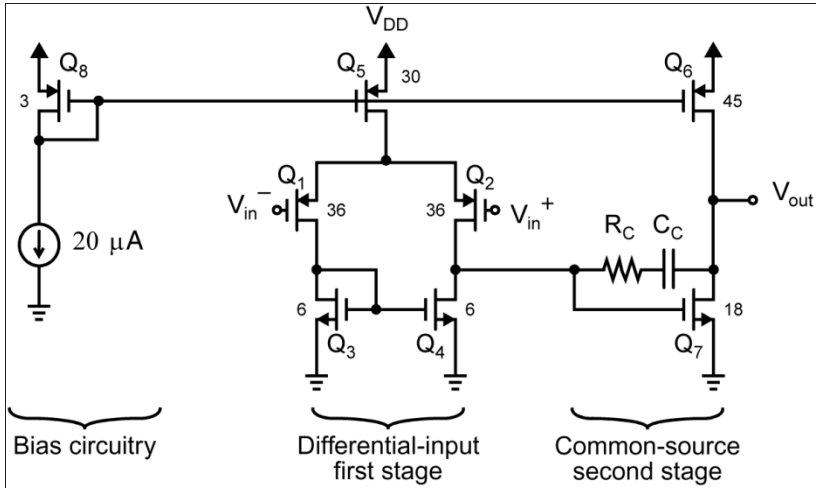
$$I_{D8} = 20\ \mu A, \quad I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D5}/2 = (W_5/2W_8)I_{D8} = 100\ \mu A$$

$$I_{D6} = I_{D7} = (W_6/W_5)I_{D5} = 300\ \mu A$$

$$g_{m1} = g_{m2} = 1.30\ mA/V, \text{ and } g_{m7} = 3.12\ mA/V.$$

$$r_{ds} = \frac{1}{\lambda I_{D\text{-sat}}} \cong \frac{1}{\lambda I_D} \qquad r_{ds1} = r_{ds2} = r_{ds3} = r_{ds4} = 37.5\ k\Omega \qquad r_{ds6} = r_{ds7} = 12.5\ k\Omega$$

$$A_{v1} = -g_{m1}(r_{ds2} \| r_{ds4}) = -24.4\ V/V \qquad A_{v2} = -g_{m7}(r_{ds6} \| r_{ds7}) = -19.5\ V/V$$



Chapter 6 Figure 03

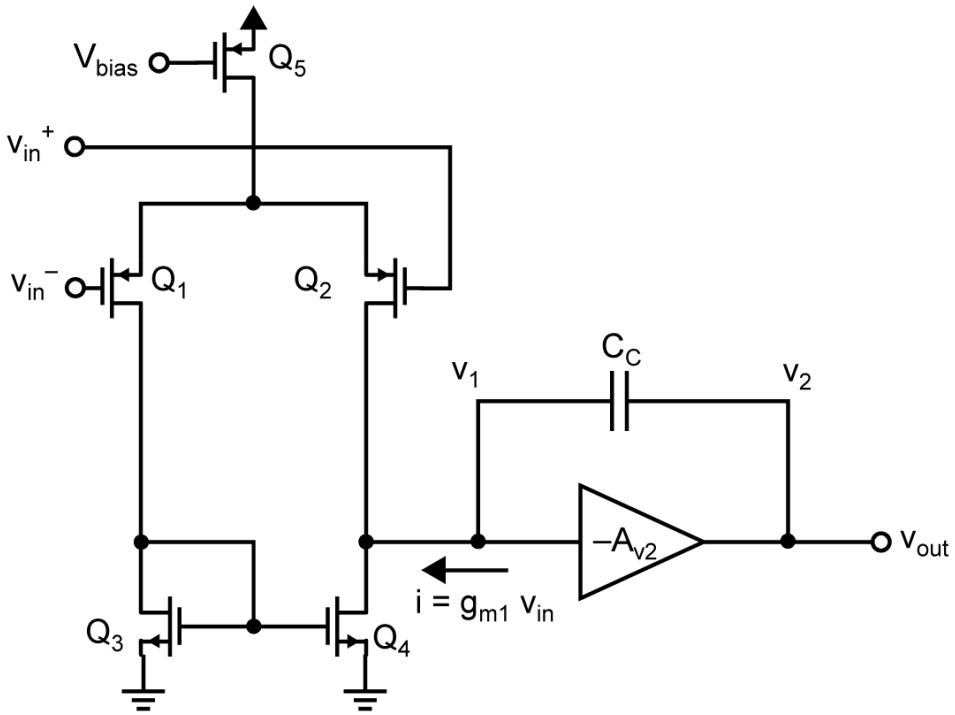
It should be noted again that the hand calculation using the approximate equations above is of only moderate accuracy, especially the output resistance calculation on r_{ds}. Therefore, later they should be verified by simulation by SPICE/SPECTRE.

However, the benefit of performing a hand calculation is to give an initial (hopefully good) design and also see what parameters affect the gain.

6.1.2 Frequency response: first order model

At frequencies where the comp. capacitor Cc has caused the gain to decrease, but still at frequencies well below the unity-gain frequency of the OpAmp. This is typically referred to as Midband frequencies for many applications.

At these frequencies, we can make some simplifying assumptions. First, ignore all other capacitors xcept Cc, which typically dominates in these frequencies. Second, temporarily neglect Rc, which has an effect only around the unity-gain freq. of the OpAmp. The resulting simplified circuit is shown below.



Chapter 6 Figure 04

6.1.2 Frequency response: first order model

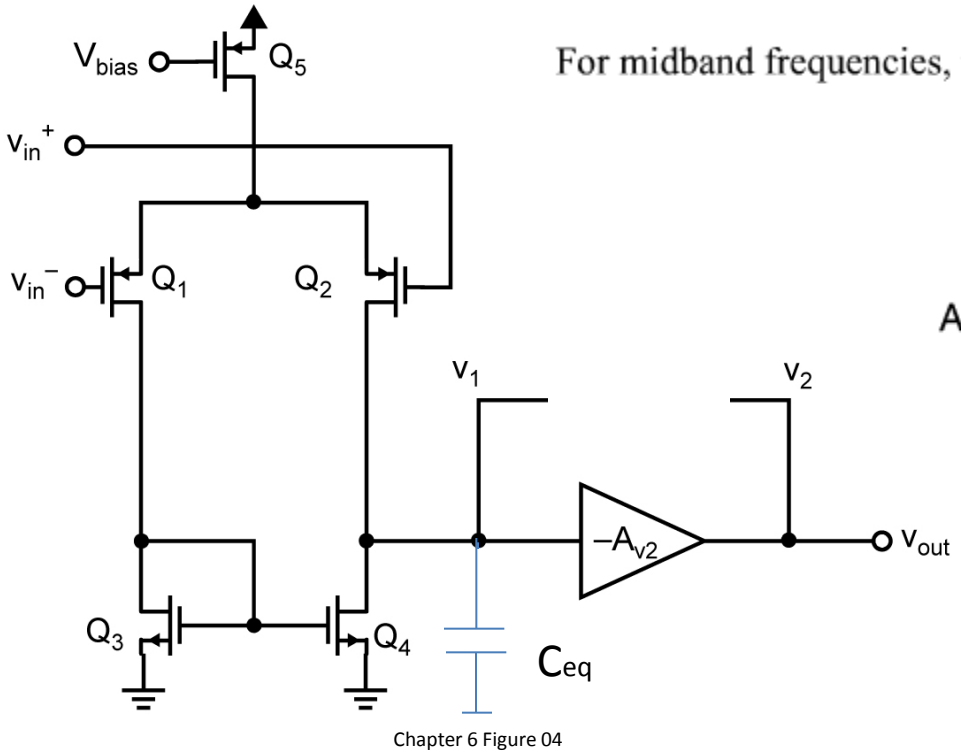
The second stage introduces primarily a capacitive load on the first stage due to the compensation capacitor, C_C. Using Miller's theorem (Section 4.2.3), one can show that the equivalent load capacitance, C_{eq}, at node v_1 is given by

$$C_{eq} = C_C(1 + A_{v2}) \approx C_C A_{v2} \tag{6.4}$$

The gain in the first stage can now be found using the small-signal model of Figure 4.37, resulting in

$$A_{v1} = \frac{v_1}{v_{in}} = -g_{m1} Z_{out1} \tag{6.5}$$

$$Z_{out1} = r_{ds2} \parallel r_{ds4} \parallel \frac{1}{sC_{eq}}$$



Chapter 6 Figure 04

For midband frequencies, the impedance of C_{eq} dominates, and we can write

$$Z_{out1} \cong \frac{1}{sC_{eq}} \cong \frac{1}{sC_C A_{v2}}$$

$$A_v(s) \equiv \frac{v_{out}}{v_{in}} = A_{v2}A_{v1} \cong A_{v2}\frac{g_{m1}}{sC_C A_{v2}} = \frac{g_{m1}}{sC_C}$$

Using the above equation, we can approximate the Unity-Gain frequencv as follows:

$$\omega_{ta} \cong \frac{g_{m1}}{C_C} = \frac{2I_{D1}}{V_{eff1}C_C} = \frac{I_{D5}}{V_{eff1}C_C}$$

For a fixed w_{ta}, power consumption is minimized by small I_D, therefore small V_{eff1}.

6.1.2 Frequency response: second order model

In the second-order model, it is assumed that any parasitic poles in the first stage are at frequencies much higher than the w_{ta} and can therefore be ignored (except at the node V1).

$$R_1 = r_{ds4} \| r_{ds2}$$

$$C_1 = C_{db2} + C_{db4} + C_{gs7}$$ C_{gd2} and C_{gd4} may be included

$$R_2 = r_{ds6} \| r_{ds7}$$

$$C_2 = C_{db7} + C_{db6} + C_{L2}$$ C_{gd6} may be included (C_{gd7} may be lumped to C_c)

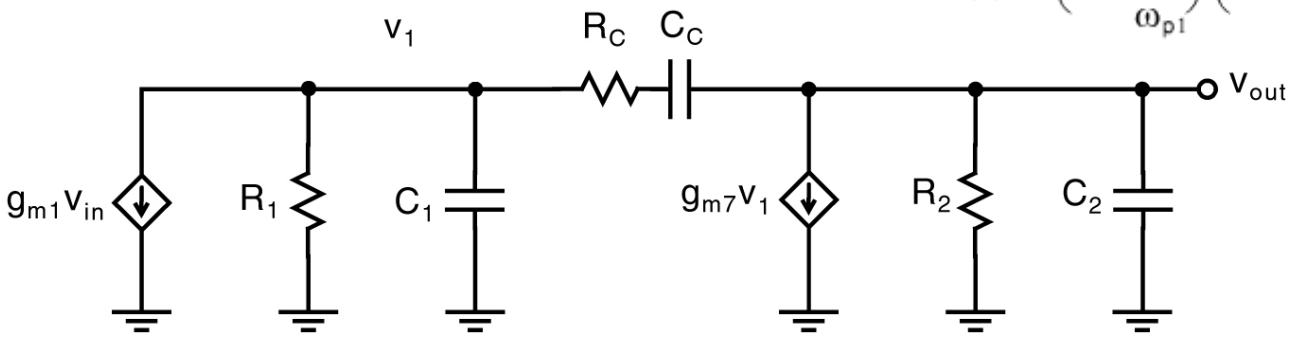
Assume Rc=0 at first, then

$$A_v(s) = \frac{v_{out}}{v_{in}} = \frac{g_{m1}g_{m7}R_1R_2\left(1 - \frac{sC_C}{g_{m7}}\right)}{1 + sa + s^2b}$$

$$a = (C_2 + C_C)R_2 + (C_1 + C_C)R_1 + g_{m7}R_1R_2C_C \qquad b = R_1R_2(C_1C_2 + C_1C_C + C_2C_C)$$

Assume that the two poles are widely separated, then the denom. of $A_v(s)$ is

$$D(s) = \left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right) \cong 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1}\omega_{p2}}$$



Chapter 6 Figure 05

6.1.2 Frequency response: second order model

The dominant pole, ω_{p1}, is given by

$$\omega_{p1} \cong \frac{1}{R_1[C_1 + C_C(1 + g_{m7}R_2)] + R_2(C_2 + C_C)}$$

$$\cong \frac{1}{R_1C_C(1 + g_{m7}R_2)}$$

$$\cong \frac{1}{g_{m7}R_1R_2C_C}$$

nondominant pole, ω_{p2}, is given by

$$\omega_{p2} \cong \frac{g_{m7}C_C}{C_1C_2 + C_2C_C + C_1C_C}$$

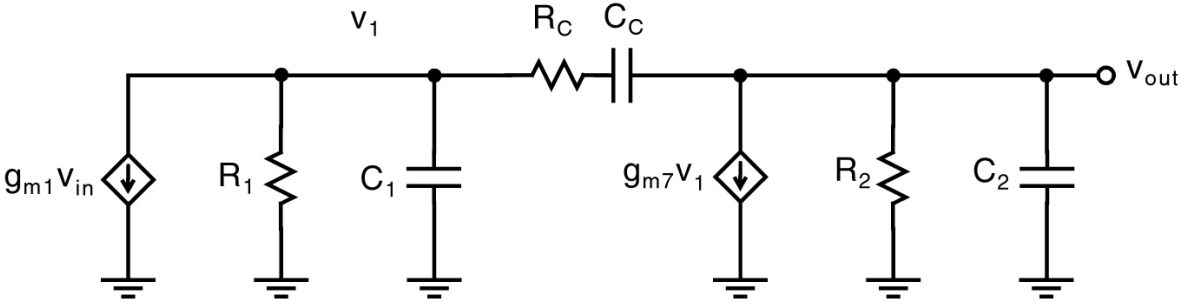
$$\cong \frac{g_{m7}}{C_1 + C_2}$$

zero, ω_z, is located in the right half plane and is given by

$$\omega_z = \frac{-g_{m7}}{C_C}$$

From the two poles, increasing g_{m7} is good to separate them more; also increasing C_c makes w_{p1} smaller. Both make the OpAmp more stable.

However, a problem arises from the zero, as it gives negative phase shift in the transfer function, which makes stability difficult. Making C_c large does not help as w_z will reduce too. Increasing g_{m7} helps at the cost of power. $W_{ta}<0.5w_{p2}$ for 65 degrees of phase margin.



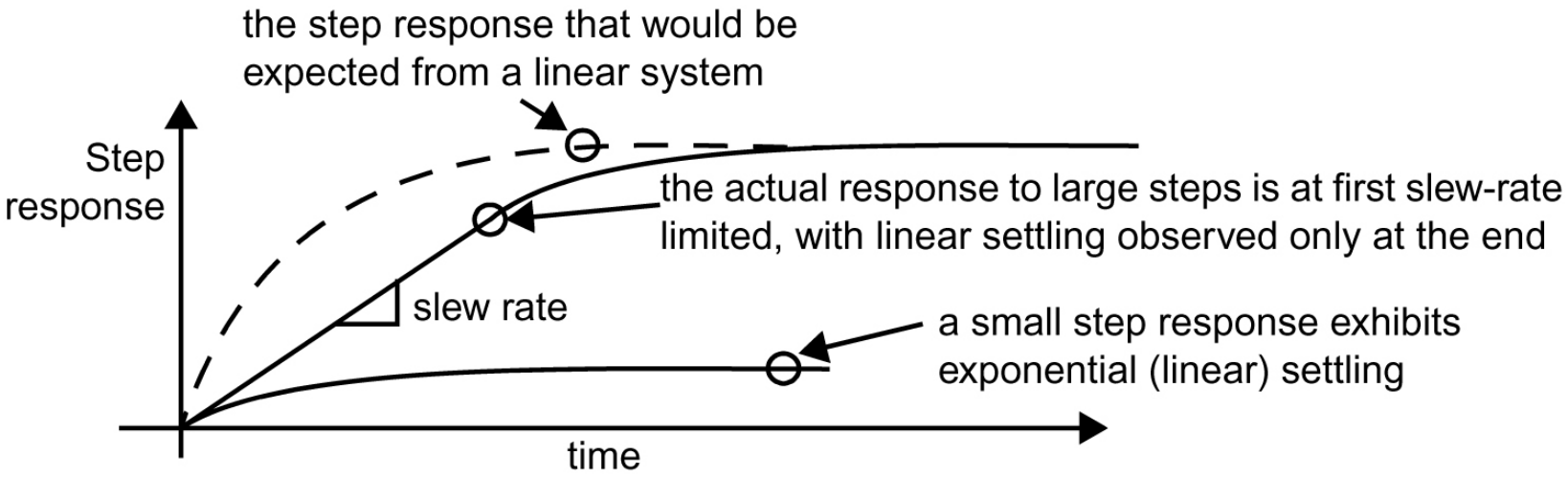
Chapter 6 Figure 05

6.1.3 Slew rate

The maximum rate at which the output of an OpAmp can change is limited by the finite bias current.

When the inputs change too quickly the OpAmp's output voltage changes at its maximum rate, called slew rate. In this case, the OpAmp's response is nonlinear until it is able to resume linear operation without exceeding the slew rate.

Such transient behavior is common in switched-capacitor circuits, where the slew rate is a major factor determining the circuit's setting time.



Chapter 6 Figure 06

Example 6.4 (page 249)

Consider a closed-loop feedback amplifier with a first-order linear settling time constant of $\tau = 0.2\ \mu s$ and a slew rate of 1 V/μs. What is the time required for the output to settle when generating to a 10-mV step output with 0.1 mV accuracy? What about a 1-V step output?

The amplifier will slew-rate limit whenever the slope demanded by linear settling exceeds the maximum imposed by slew-rate limiting. For a step height V_{step}, linear settling is exponential.

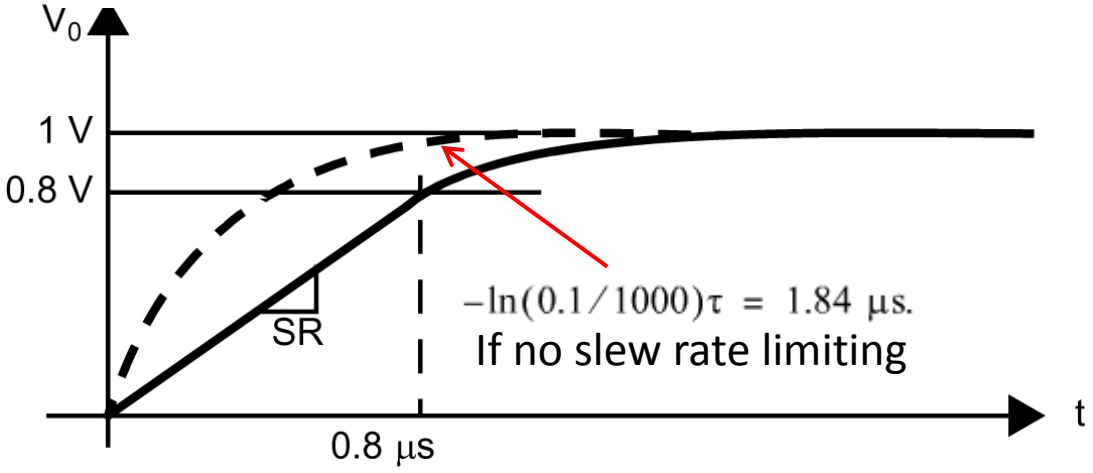
$$v_o = V_{step}(1 - e^{-t/\tau}) \tag{6.22}$$

The highest rate of change is observed right at the time of the step.

$$\left.\frac{dv_o}{dt}\right|_{max} = \left.\frac{dv_o}{dt}\right|_{t=0} = \frac{V_{step}}{\tau} \tag{6.23}$$

So long as this maximum slope is less than the slew rate, slew-rate limiting is avoided. Hence, the maximum step size that can be tolerated without slew-rate limiting is

$$V_{step,\,max} < SR \cdot \tau = 0.2V \tag{6.24}$$



Chapter 6 Figure 07

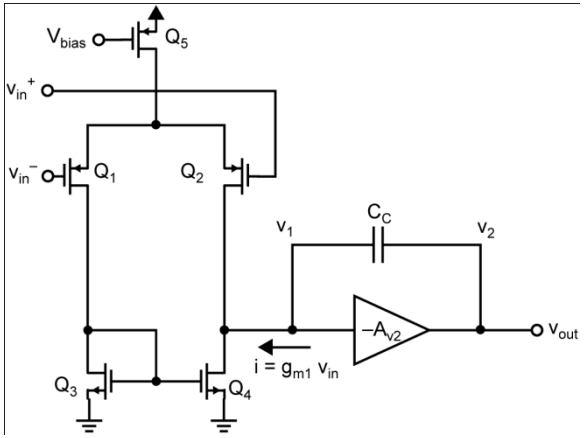
Case 1: $4.6\tau = 0.92\ \mu s.$

Case 2: note that linear settling starts when output Vo reaches 0.8V. Initially slew rate for (1-0.2)/SR=0.8us, then it needs another $-\ln(0.1/200) = 7.6$ time constants. So total

$$0.8\ \mu s + 7.6\tau = 2.32\ \mu s.$$

6.1.3 Slew rate

When the opamp of Fig. 6.3 is limited by its slew rate because a large input signal is present, all of the bias current of Q_5 goes into either Q_1 or Q_2, depending on whether v_{in} is negative or positive. When v_{in} is a large positive voltage, the bias current, I_{D5}, goes entirely through Q_1 and also goes into the current-mirror pair, Q_3, Q_4. Thus, the current coming out of the compensation capacitor, C_C, (i.e., I_{D4}) is simply equal to I_{D5} since Q_2 is off. When v_{in} is a large negative voltage, the current-mirror pair Q_3 and Q_4 is shut off because Q_1 is off, and now the bias current, I_{D5}, goes directly into C_C. In either case, the maximum current entering or leaving C_C is simply the total bias current, I_{D5}.[7] (In fact, it requires the $I_{D6}>I_{D5}$)



Chapter 6 Figure 04

$$SR \equiv \left.\frac{dv_{out}}{dt}\right|_{max} = \frac{I_{C_C}|_{max}}{C_C} = \frac{I_{D5}}{C_C} = \frac{2I_{D1}}{C_C}$$

From first order model

$$\omega_{ta} = \frac{g_{m1}}{C_C} \longrightarrow SR = \frac{2I_{D1}\omega_{ta}}{g_{m1}}$$

$$g_{m1} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}} \longrightarrow SR = \frac{2I_{D1}}{\sqrt{2\mu_p C_{ox}(W/L)_1 I_{D1}}}\omega_{ta} = V_{eff1}\omega_{ta}$$

$$V_{eff1} = \sqrt{\frac{2I_{D1}}{\mu_p C_{ox}(W/L)_1}}$$

Since stability demands that ω_{ta} be lower than ω_{p2}, *the only ways of improving the slew rate for a properly-compensated two-stage CMOS opamp is to increase* V_{eff1} *or* ω_{p2}.

Assuming a fixed power consumption, and hence fixed bias currents, increasing V_{eff1} improves the slew rate (6.30) and helps to minimize distortion, but also lowers the transconductance of the input stage which decreases the dc gain (6.1), and increases the equivalent input thermal noise (see Chapter 9).

6.1.4 nMOS or pMOS input stage?

The choice depends on a number of tradeoffs.

First, the gain does not seem to be affected much to first order.

Second, have pMOS input stage allows the second stage be nMOS common-source amplifier to that its g_m can be maximized when high frequency operation is important, as both w_{p2} and w_{ta} are proportional to g_m. (g_m of nMOS is larger under the same current and size).

Third, if the third stage of source follower is needed, then an nMOS version is preferable as this will have less voltage drop. (but it is not used when there is only capacitive load).

Fourth, noise is a concern. Typically, pMOS helps reduce the noise.

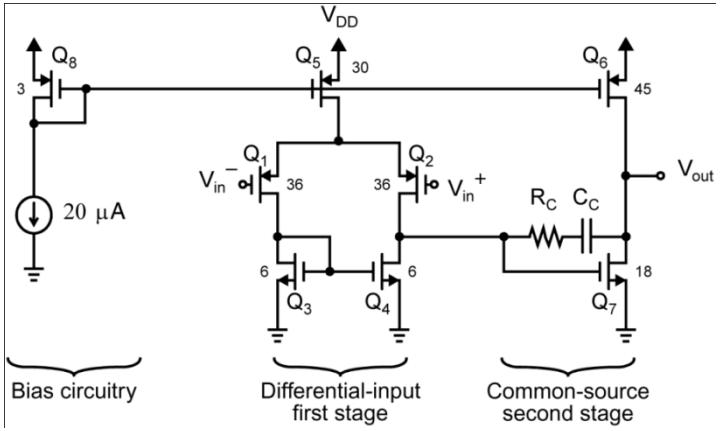
In summary, when using a two-stage OpAmp, the pMOS input stage is preferred to optimize w_{ta} and minimize noise.

6.1.5 Systematic offset voltage

When designing two-stage OpAmp, the sizes of transistor has to be carefully set to avoid inherent or systematic input offset voltage.

When input differential voltage is 0, V_{GS7} should be what is required to make I_{D7} equal to I_{D6}.

$$V_{GS7} = \sqrt{\frac{2I_{D6}}{\mu_n C_{ox}(W/L)_7}} + V_{tn}$$



Chapter 6 Figure 03

Also, note that $V_{GS7} = V_{DS3} = V_{GS4}$

$$V_{GS4} = \sqrt{\frac{2I_{D4}}{\mu_n C_{ox}(W/L)_4}} + V_{tn}$$

$$\sqrt{\frac{2I_{D4}}{\mu_n C_{ox}(W/L)_4}} = \sqrt{\frac{2I_{D6}}{\mu_n C_{ox}(W/L)_7}} \longrightarrow \frac{I_{D4}}{(W/L)_4} = \frac{I_{D6}}{(W/L)_7}$$

Also $$\frac{I_{D6}}{I_{D4}} = \frac{I_{D6}}{I_{D5}/2} = \frac{(W/L)_6}{(W/L)_5/2}$$

Finally we see that the necessary condition to ensure that no input-offset voltage is present is

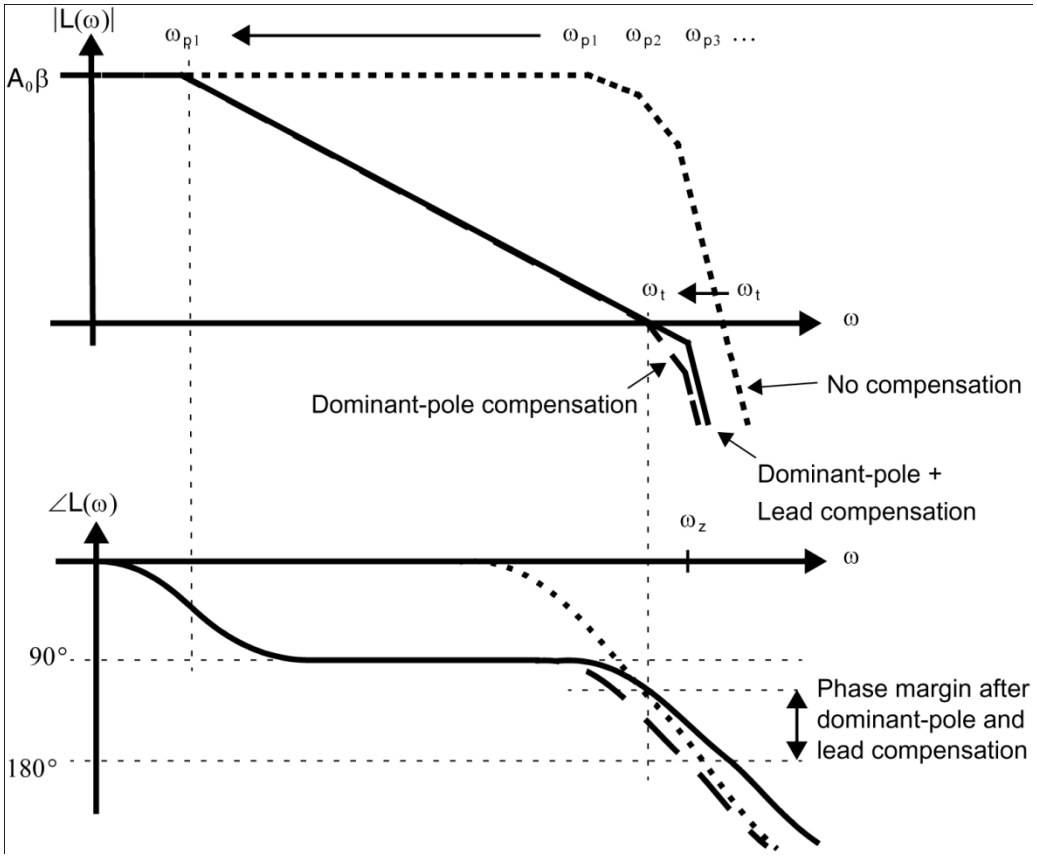
$$\frac{(W/L)_7}{(W/L)_4} = 2\frac{(W/L)_6}{(W/L)_5}$$

By meeting these constraints, one can achieve a smaller offset voltage (it may still exist due to mis-match of transistors).

6.2 OpAmp compensation

Optimal compensation of OpAmps may be one of the most difficult parts of design. Here a systematic approach that may result in near optimal designs are introduced that applies to many other OpAmps.

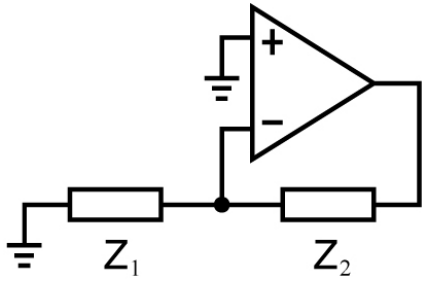
Two most popular approaches are dominant-pole compensation and lead compensation.



Chapter 6 Figure 08

A further increase in phase margin is obtained by lead compensation which introduces a left half plane zero at a frequency slightly greater than the unity gain frequency w_t. If done properly, this has minimal effect on w_t but gives an additional 20-30 degrees of phase margin.

6.2.2. Dominant pole compensation



Chapter 6 Figure 09

$$L(s) \approx A_v(s)\frac{Z_1}{Z_1 + Z_2}$$

The capacitor, C_C, controls the dominant first pole, (i.e., ω_{p1}), and thereby the loop's unity-gain frequency, ω_t.

$$\omega_t = L_0\omega_{p1} = \beta g_{m1}/C_C \qquad (6.42)$$

Hence, by properly selecting the value of C_C dominant-pole compensation can be achieved.

Especially if the load capacitor C_L dominants so that the second pole w_{p2} is relatively constant when C_c changes (see slide 10).

$$\omega_{p1} \cong \frac{1}{R_1[C_1 + C_C(1 + g_{m7}R_2)] + R_2(C_2 + C_C)} \cong \frac{1}{R_1C_C(1 + g_{m7}R_2)} \cong \frac{1}{g_{m7}R_1R_2C_C}$$

$$\omega_{p2} \cong \frac{g_{m7}C_C}{C_1C_2 + C_2C_C + C_1C_C} \cong \frac{g_{m7}}{C_1 + C_2}$$

$$\omega_z = \frac{-g_{m7}}{C_C}$$

6.2.2. Lead compensation

$$\omega_{p1} \cong \frac{1}{R_1[C_1 + C_C(1 + g_{m7}R_2)] + R_2(C_2 + C_C)} \cong \frac{1}{R_1 C_C(1 + g_{m7}R_2)} \cong \frac{1}{g_{m7}R_1R_2C_C}$$

$$\omega_{p2} \cong \frac{g_{m7}C_C}{C_1C_2 + C_2C_C + C_1C_C} \cong \frac{g_{m7}}{C_1 + C_2}$$

$$\omega_z = \frac{-g_{m7}}{C_C}$$

Lead compensation is achieved using R_C. If the small-signal model of Fig. 6.5 is reanalyzed with a nonzero R_C, then a third-order denominator results. The first two poles are still approximately at the frequencies given by (6.19) and (6.20). The third pole is at a high frequency and has almost no effect. However, the zero is now determined by the relationship

$$\omega_z = \frac{-1}{C_C(1/g_{m7} - R_C)}$$

This results in a number of design opportunities:

1. One could take $R_C = 1/g_{m7}$
2. One can make Rc larger so that w_z cancels the non-dominant pole (pole-zero canceling), this requires: $R_C = \frac{1}{g_{m7}}\left(1 + \frac{C_1 + C_2}{C_C}\right)$

Unfortunately, C_2 is often not known a priori, especially when no output stage is present.

3. The third way is to take Rc even larger so that it is slightly larger than the unity gain frequency that would results if the lead resistor were not present. For example, if the new w_z is 70% higher than w_t $\omega_z = 1.7\omega_t$ it will introduce a phase lead of $\tan^{-1}(1/1.7) = 30°$.

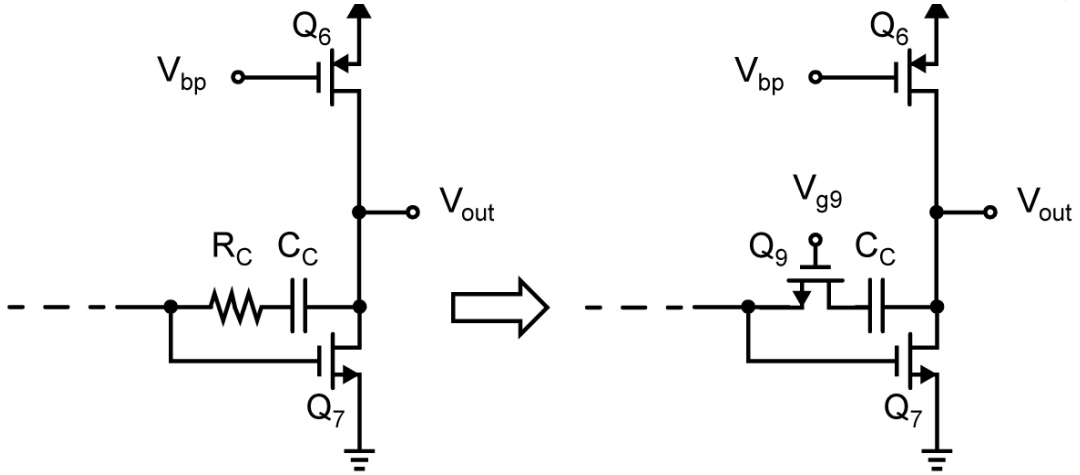
Assuming $R_C >> (1/g_{m7})$, then $\omega_z \cong 1/(R_C C_C)$. Recall $\omega_t = \beta g_{m1}/C_C$,

choose R_C according to $R_C \cong \frac{1}{1.7\beta g_{m1}}$

6.2.2. Lead compensation

Finally, the lead compensation resistor R_C may be replaced by a transistor operating in the triode region, as illustrated in Fig. 6.10. Transistor Q_9 has $V_{DS9} = 0$ since no dc bias current flows through it, and therefore Q_9 is deep in the triode region. Thus, this transistor operates as a resistor, R_C, with a value given by

$$R_C = r_{ds9} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_9 V_{eff9}} \tag{6.48}$$



It should be noted here that r_{ds} indicates the drain-source resistance of Q_9 when it is in the triode region as opposed to the finite-output impedance of Q_9 when it is in the active mode. The same notation, r_{ds}, is used to indicate the drain-source resistance in both cases—whether the transistor is in the active or the triode region. One simply has to check which region a transistor is operating in to ensure that the correct equation is used to determine r_{ds}.

6.2.2. Summary of Lead compensation

This approach leads to the following design procedure for compensation of a two-stage CMOS opamp:

$$\omega_t = L_0\omega_{p1} = \beta g_{m1}/C_C$$

$$\omega_{p2} \cong \frac{g_{m7}C_C}{C_1C_2 + C_2C_C + C_1C_C} \cong \frac{g_{m7}}{C_1 + C_2}$$

1. Start by choosing, somewhat arbitrarily, $C_C' \cong (\beta g_{m1}/g_{m7})C_L$. This initially places the loop's unity gain frequency (6.42) approximately at the frequency of the second pole (6.20), where it has been assumed that the load capacitance C_L is dominant.
2. Using SPICE, find the frequency at which a $-125°$ phase shift exists. Let the gain at this frequency be denoted A'. Also, let the frequency be denoted ω_t. This is the frequency that we would like to become the unity-gain frequency of the loop gain.
3. Choose a new C_C so that ω_t becomes the unity-gain frequency of the loop gain, thus resulting in a $55°$ phase margin. (Obtaining this phase margin is the reason we chose $-125°$ in step 2.) This can be achieved by taking C_C according to the equation

$$C_C = C_C'A' \quad (6.49)$$

This make w_t smaller while w_{p2} relatively constant if C_L dominates

It might be necessary to iterate on C_C a couple of times using SPICE.

4. Choose R_C according to

$$R_C = \frac{1}{1.7\omega_t C_C} \quad (6.50)$$

This choice will increase the phase margin approximately $30°$ resulting in a total phase margin of approximately $85°$. It allows a margin of $5°$ to account for processing variations without the poles of the closed-loop response becoming real. *This choice is a lso almost optimum lead compensation for almost any opamp when a resistor is placed in series with the compensation capacitor.* It might be necessary to iterate on R_C

5. If, after step 4, the phase margin is not adequate, then increase C_C while leaving R_C constant. This will move both ω_t and the lead zero to lower frequencies while keeping their ratio approximately constant, thus minimizing the effects of higher-frequency poles and zeros which, hopefully, do not also move to lower frequencies. In most cases, the higher-frequency poles and zeros (except for the lead zero) will not move to significantly lower frequencies when C_C is increased.
6. The final step is to replace R_C by a transistor. The size of the transistor can be chosen using equation (6.48), which is repeated here for convenience:

$$R_C = r_{ds9} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_9 V_{eff9}} \tag{6.51}$$

Finally, SPICE can be used again to fine-tune the device dimensions to optimize the phase margin to that obtained in steps 4 and 5.

Example 6.7 (page 258)

An opamp has an open-loop transfer function given by

$$A(s) = \frac{A_0(1 + s/\omega_z)}{(1 + s/\omega_{p1})(1 + s/\omega_2)} \tag{6.52}$$

Here, A_0 is the dc gain of the opamp and ω_z, ω_p, and ω_2 are the frequencies of a zero, the dominant pole, and the equivalent second pole, respectively. Assume that $\omega_2 = 2\pi \times 50$ MHz and that $A_0 = 10^4$. The opamp is to be used in a unity-gain configuration so that $\beta = 1$ and $L(s) = A(s)$.

a. Assuming $\omega_z \to \infty$, find ω_{p1} and the unity-gain frequency, ω_t', so that the opamp has a unity-gain phase margin of 55°.

b. Assuming $\omega_z = 1.7\omega_t'$ (where ω_t' is as found in part (a)), what is the new unity-gain frequency, ω_t? Also, find the new phase margin.

$\omega >> \omega_{p1}$ $\quad L(s) = A(s) \cong \dfrac{A_0(1 + s/\omega_z)}{(s/\omega_{p1})(1 + s/\omega_2)}$

(*a*) For $\omega_z \to \infty$

$$\angle A(j\omega_t') = -90° - \tan^{-1}(\omega_t'/\omega_2) = -125°$$

$$\tan^{-1}(\omega_t'/\omega_2) = 35° \quad \Rightarrow \omega_t' = 2.2 \times 10^8 \text{ rad/s} = 2\pi \times 35 \text{ MHz}$$

$$\frac{A_0}{(\omega_t'/\omega_{p1})\sqrt{1 + (\omega_t'/\omega_2)^2}} = 1 \quad \Rightarrow \omega_{p1} = \frac{\omega_t'\sqrt{1 + (\omega_t'/\omega_2)^2}}{A_0} = 2\pi \times 4.28 \text{ kHz}$$

Or we can simply estimate w_{p1} equal to w_t'/A_0=3.5kHz

Example 6.7 (page 258)

An opamp has an open-loop transfer function given by

$$A(s) = \frac{A_0(1 + s/\omega_z)}{(1 + s/\omega_{p1})(1 + s/\omega_2)} \tag{6.52}$$

Here, A_0 is the dc gain of the opamp and ω_z, ω_p, and ω_2 are the frequencies of a zero, the dominant pole, and the equivalent second pole, respectively. Assume that $\omega_2 = 2\pi \times 50$ MHz and that $A_0 = 10^4$. The opamp is to be used in a unity-gain configuration so that $\beta = 1$ and $L(s) = A(s)$.

a. Assuming $\omega_z \to \infty$, find ω_{p1} and the unity-gain frequency, ω_t', so that the opamp has a unity-gain phase margin of 55°.

b. Assuming $\omega_z = 1.7\omega_t'$ (where ω_t' is as found in part (a)), what is the new unity-gain frequency, ω_t? Also, find the new phase margin.

$\omega >> \omega_{p1}$ $\qquad L(s) = A(s) \cong \dfrac{A_0(1 + s/\omega_z)}{(s/\omega_{p1})(1 + s/\omega_2)}$

(*b*) First, we set

$$\omega_z = 1.7\omega_t' = 2\pi \times 59.5 \text{ MHz}$$

To find the new unity-gain frequency, setting $|A(j\omega_t)| = 1$

$$\frac{A_0\sqrt{1 + (\omega_t/\omega_z)^2}}{(\omega_t/\omega_{p1})\sqrt{1 + (\omega_t/\omega_2)^2}} = 1 \quad \Rightarrow \omega_t = \frac{A_0\omega_{p1}\sqrt{1 + (\omega_t/\omega_z)^2}}{\sqrt{1 + (\omega_t/\omega_2)^2}} \qquad \omega_t = 2\pi \times 39.8 \text{ MHz}.$$

$$\angle A(j\omega_t) = -90° + \tan^{-1}(\omega_t/\omega_z) - \tan^{-1}(\omega_t/\omega_2) = -95° \qquad \text{a phase margin of } 85°$$

6.2.3 Making compensation independent of process and temperature

$$\omega_t = \frac{g_{m1}}{C_C}$$

$$\omega_{p2} \cong \frac{g_{m7}}{C_1 + C_2}$$

In a typical process, the ratios of all g_ms remain relatively constant over process and temperature variation since the g_ms are all determined by the same biasing network. (μ_n/μ_p is relatively constant tool)
Also, mostly the capacitors also track each other or remain relatively constant.

the lead zero is at a frequency given by $$\omega_z = \frac{-1}{C_C(1/g_{m7} - R_C)}$$

Thus, if R_C can also be made to track the inverse of transconductances, and in particular $1/g_{m7}$, then the lead zero will also be proportional to the transconductance of Q_7. As a result, the lead zero will remain at the same relative frequency with respect to ω_t and ω_{p2}, as well as all other high-frequency poles and zeros. In other words, the lead compensation will be mostly independent of process and temperature variations.

recall that R_C is actually realized by Q_9, and therefore we have $$R_C = r_{ds9} = \frac{1}{\mu_n C_{ox}(W/L)_9 V_{eff9}}$$

$$g_{m7} = \mu_n C_{ox}(W/L)_7 V_{eff7}$$

Thus, the product $R_C g_{m7}$, which we want to be a constant, is given by

ally realized by Q_9, and therefore we have $$R_C g_{m7} = \frac{(W/L)_7 V_{eff7}}{(W/L)_9 V_{eff9}}$$

So then we need to make sure that V_{eff9}/V_{eff7} is independent of process and temperature variations. It may be made constant by deriving V_{GS9} from the same biasing network used to derive V_{GS7}. (see the circuit in next slide)

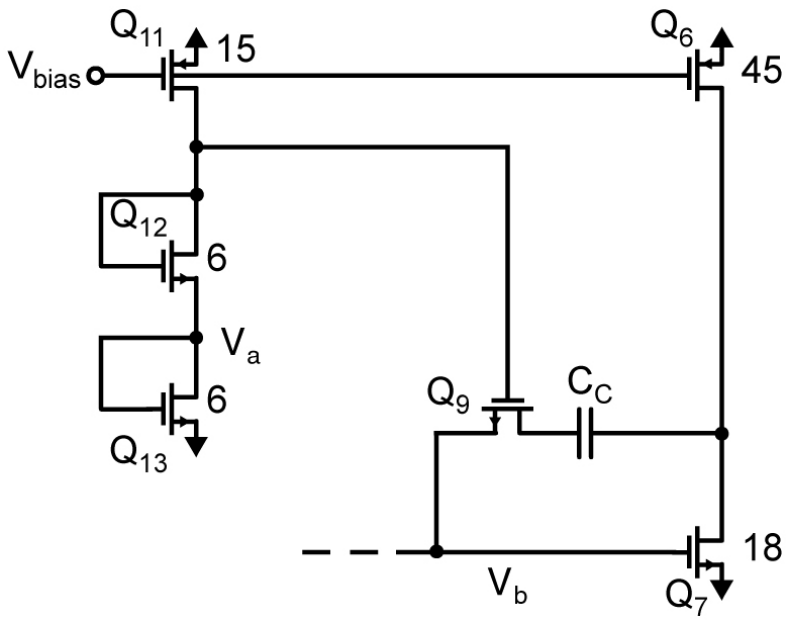
First, we need to make $V_a=V_b$, which is possible is $V_{eff13}=V_{eff7}$, i.e.

$$\sqrt{\frac{2I_{D7}}{\mu_n C_{ox}(W/L)_7}} = \sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}} \longrightarrow \frac{I_{D7}}{I_{D13}} = \frac{(W/L)_7}{(W/L)_{13}}$$

Also note the ratio I_{D7}/I_{D13} is set from the current mirror pair Q_6, Q_{11}, resulting in $\frac{I_{D7}}{I_{D13}} = \frac{(W/L)_6}{(W/L)_{11}}$

Thus, to make $V_{eff13} = V_{eff7}$, we need to satisfy the following relationship: $\frac{(W/L)_6}{(W/L)_7} = \frac{(W/L)_{11}}{(W/L)_{13}}$

The note that once $V_a=V_b$, then $V_{GS12}=V_{GS9}$, which mean $V_{eff12}=V_{eff9}$,



Chapter 6 Figure 11

$$\frac{V_{eff7}}{V_{eff9}} = \frac{V_{eff13}}{V_{eff12}} = \frac{\sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}}}{\sqrt{\frac{2I_{D12}}{\mu_n C_{ox}(W/L)_{12}}}} = \sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}}$$

$I_{D12} = I_{D13}$,

So finally, we have

$$R_C g_{m7} = \frac{(W/L)_7 V_{eff7}}{(W/L)_9 V_{eff9}} = \frac{(W/L)_7}{(W/L)_9}\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}}$$