

6.5 Current mirror OpAmp

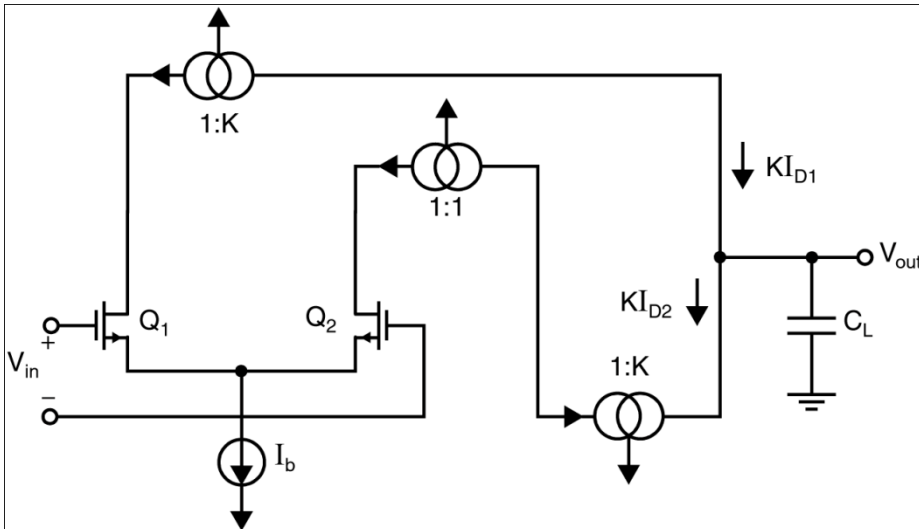
Another popular OpAmp when driving only on-chip capacitive loads is the current-mirror OpAmp. Note that at the Q2 side, more current mirrors needs to be used to provide current $K_{D2}=K_{D1}$.

Also, it can be seen that all internal nodes have low impedance except the output node. By using proper current mirrors with high output impedance, good gain can be achieved.

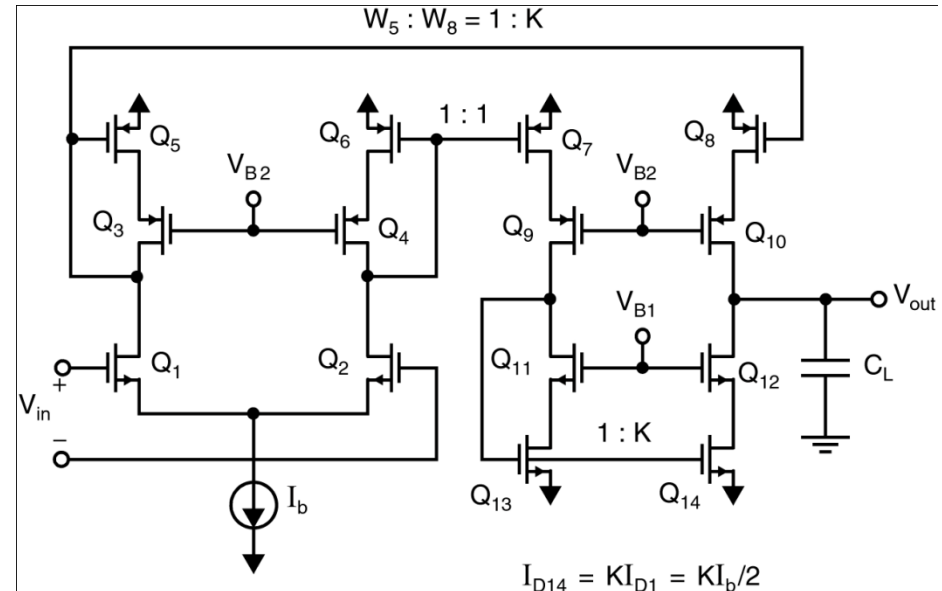
The overall transfer function of this OpAmp closely approximate dominant-pole operation.

$$A_V = \frac{V_{out}(s)}{V_{in}(s)} = K_{g_{m1}} Z_L(s) = \frac{K_{g_{m1}} r_{out}}{1 + s r_{out} C_L} \approx \frac{K_{g_{m1}}}{s C_L}$$

$$\text{unity-gain frequency } \omega_{\text{ta}} = \frac{K g_{m1}}{C_L} = \frac{2 K I_{D1}}{C_L V_{\text{eff},1}}$$



Chapter 6 Figure 21



Chapter 6 Figure 22

If the power dissipation is specified, the total current, $I_{\text{total}} = (3 + K)I_{D1}$ $\longrightarrow \omega_{\text{ta}} = \frac{K}{(3 + K)} \frac{2I_{\text{total}}}{V_{\text{eff},1} C_L}$

It can be seen that larger K increases the unity-gain frequency assuming the load capacitor dominates the time constants. Larger K also increases the gain. A typical upper limit for K is 5.

A detailed analysis reveals important nodes for determining the non-dominant poles, at the drain of Q1 first and drain of Q2 and Q9 secondly. Larger K increases the capacitances at these nodes while also increases the resistance (assuming a fixed I_{total}), which reduce the non-dominant poles. In this case, then C_L has to be increased to maintain a large phase margin. So, K should not be too large, i.e. $K \leq 2$ usually.

During slew rate, all of the bias current I_b of the first stage is diverted through Q1/2 and amplified by the current mirror gain to the output. The total current to charge/discharge the load is KI_b . So the slew rate is $SR = \frac{KI_b}{C_L}$

Due primarily to the larger unity-gain frequency and slew rate, the current-mirror OpAmp may be preferred over the folded-cascode OpAmp. However, one has to be careful that the current-mirror OpAmp has larger input noise as well, as its input stage is biased at a lower portion of the total bias current and therefore a relatively smaller g_m given the same power consumption.

Example 6.11 (page 277)

Assume the current-mirror opamp shown in Fig. 6.22 has all transistor lengths equal to $0.4\text{ }\mu\text{m}$ and transistor widths as given in Table 6.2. Notice that $K = 2$. Assume the process parameters for the $0.18\text{-}\mu\text{m}$ process in Table 1.5, a single 1.8-V power supply, and that the opamp's total current dissipation is 0.4 mA . The load capacitance is $C_L = 2.5\text{ pF}$.

Q_1	90/0.4	Q_7	20/0.4	Q_{13}	4/0.4
Q_2	90/0.4	Q_8	40/0.4	Q_{14}	8/0.4
Q_3	20/0.4	Q_9	20/0.4		
Q_4	20/0.4	Q_{10}	40/0.4		
Q_5	20/0.4	Q_{11}	4/0.4		
Q_6	20/0.4	Q_{12}	8/0.4		

Find the slew rate and the unity-gain frequency, assuming the equivalent second pole does not dominate. Estimate the equivalent second pole. Would it be necessary to increase C_L if a 75° phase margin were required with $\beta = 1$ and without using lead compensation? What if lead compensation were used?

$$I_b = \frac{2I_{\text{total}}}{(3 + K)} = \frac{2(0.4\text{ mA})}{(3 + K)} = 160\text{ }\mu\text{A}$$

V_{eff1} can be estimated to be about 50mV so that $g_{m1}=3.14\text{mA/V}$ is sort of maximized.

$$\omega_{ta} = \frac{Kg_{m1}}{C_L} = 1.6 \times 10^9\text{ rad/s} \Rightarrow f_{ta} = 255\text{ MHz} \quad \text{SR} = \frac{KI_b}{C_L} = 128\text{ V}/\mu\text{s}$$

Comparing to the previous example on FC-OpAmp with the same power and load, the current-mirror OpAmp can have better bandwidth and SR if K is made larger.

The dominant node almost certainly will occur at the drain of Q_1 . The impedance at this node is given by

$$R_1 = 1/g_{m5} = 1.3\text{ k}\Omega$$

the capacitance will be primarily due to the gate-source capacitances of Q_5 and Q_8 .

$$C_1 = C_{gs5} + C_{gs8} = (1 + K)C_{gs5} = (1 + K)(2/3)C_{ox}W_5L_5 = 0.14\text{ pF}$$

the time constant for this node is given by

$$\tau_1 = R_1 C_1 = 0.18 \text{ ns}$$

In a similar manner, we can calculate the impedances and, hence, the time constant for the drain of Q_2 to be $R_2 = 1.3 \text{ k}\Omega$, $C_2 = 0.091 \text{ pF}$, and $\tau_2 = R_2 C_2 = 0.12 \text{ ns}$. The other important time constant comes from the parasitic capacitors at the drain of Q_9 . Here, we have

$$R_3 = 1/g_{m13} = 1.5 \text{ k}\Omega \quad C_3 = C_{gs13} + C_{gs14} = (1 + K)(2/3)C_{ox} W_{13} L_{13} = 0.027 \text{ pF} \quad \tau_3 = 0.04 \text{ ns.}$$

The time constant of the equivalent second pole can now be estimated to be given by

$$\tau_{2eq} = \tau_1 + \tau_2 + \tau_3 = 0.34 \text{ ns} \quad p_{2eq} = \frac{1}{\tau_{2eq}} = 2.94 \times 10^9 \text{ rad/s} = 2\pi \times 468 \text{ MHz}$$

If 75 degrees of phase margin is used, the unity-gain frequency must be 0.27 times of p_{2eq} or 126MHz , so the C_L must be increased from 2.5pF to 5pF to reduce from 255MHz to 126MHz.

If lead compensation is used, then unity-gain frequency can be designed to be 0.7 times of p_{2eq} so that 55 degrees of phase margin is achieved. Then, lead compensation can be used to achieve another 20 to 30 degrees of phase margin. Also, no additional load capacitance is necessary, which reduces the circuit area.

6.6 Linear settling time revisited

We saw in Chapter 5 that the time constant for linear settling time was equal to the inverse of $\omega_{-3\text{ dB}}$ for the closed-loop circuit gain. We also saw that $\omega_{-3\text{ dB}}$ is given by the relationship

$$\omega_{-3\text{ dB}} = \omega_t \quad (6.137)$$

However, while for the classical two-stage CMOS opamp the unity-gain frequency remains relatively constant for varying load capacitances, the unity-gain frequencies of the folded-cascode and current-mirror amplifiers are strongly related to their load capacitance. As a result, their settling-time performance is affected by both the feedback factor as well as the effective load capacitance.

classical two-stage CMOS opamp	$\omega_{ta} = \frac{g_{m1}}{C_C}$
folded-cascode opamp,	$\omega_{ta} = \frac{g_{m1}}{C_L}$
a current-mirror opamp,	$\omega_{ta} = \frac{Kg_{m1}}{C_L}$

Recall from Chapter 5 the 3db bandwidth of the closed loop amplifier is the unity-gain frequency of the loop gain, which is β times the unity-gain frequency of the OpAmp, i.e.

$$\omega_t = \beta\omega_{ta}:$$

6.6 Linear settling time revisited

To determine the -3-dB frequency of a closed-loop opamp, consider the general case shown in Fig. 6.23. At the opamp output, C_{load} represents the capacitance of the next stage that the opamp must drive, while C_C is a compensation capacitance that might be added to maintain a sufficient phase margin.

At the input side, C_p represents parasitic capacitance due to large transistors at the opamp input as well as any switch capacitance

recall from Chapter 5 on negative feedback

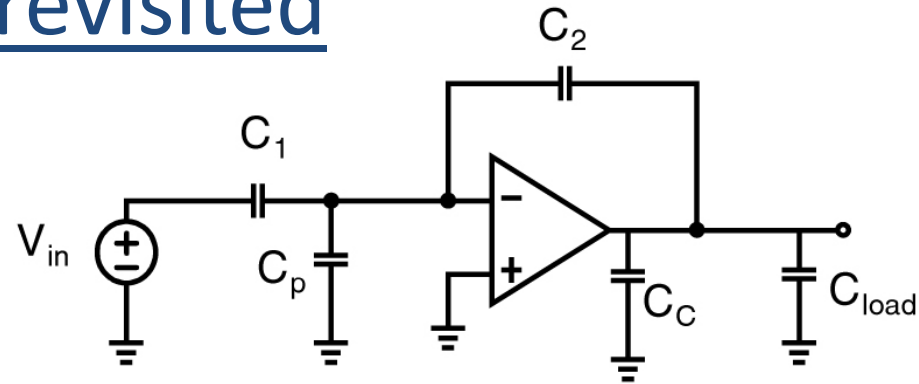
$$\beta = \frac{1/[s(C_1 + C_p)]}{1/[s(C_1 + C_p)] + 1/(sC_2)} = \frac{C_2}{C_1 + C_p + C_2}$$

The load capacitance is more complicated. Treating the inverting terminal of OpAmp open, the effective C_L is more than just C_{load} and C_C , but

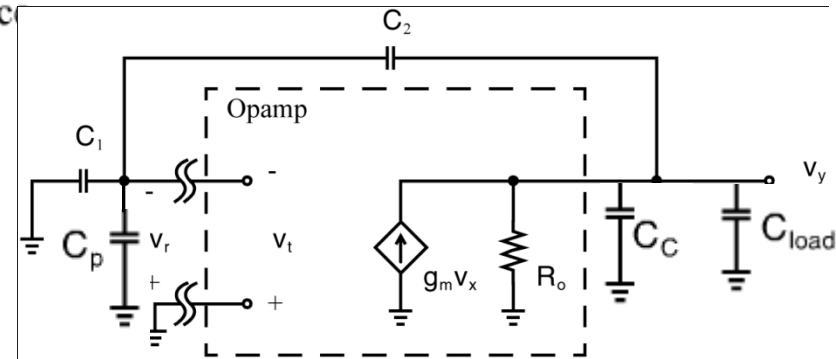
$$C_L = C_C + C_{\text{load}} + \frac{C_2(C_1 + C_p)}{C_1 + C_p + C_2}$$

This can be verified using the loop gain method introduced in Chapter 5: we can find out the loop gain first and directly find the unity-gain frequency of the loop gain:

$$V_r = -g_m V_t \frac{1}{s \left[\frac{(C_1 + C_p)C_2}{C_1 + C_p + C_2} + C_L + C_C \right]} \frac{C_2}{C_1 + C_p + C_2}$$



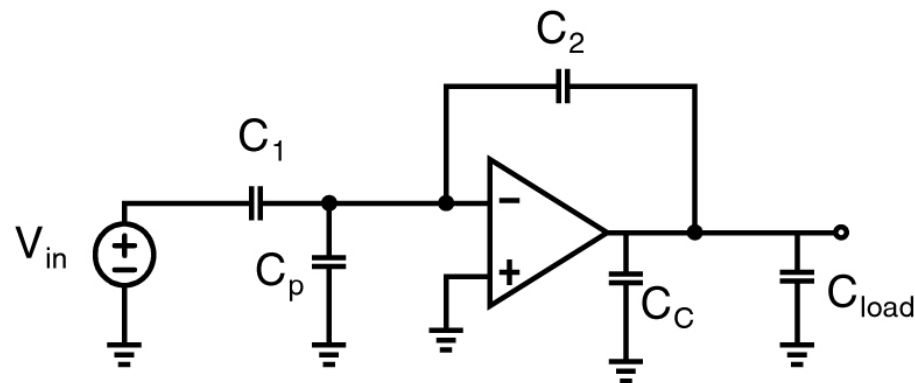
Chapter 6 Figure 23



Chapter 5 Figure 21

Example 6.12 (page 280)

Consider the current-mirror opamp with no lead compensation in Example 6.11 being used in the circuit shown in Fig. 6.23 with $C_1 = C_2 = C_C = C_{\text{load}} = 5 \text{ pF}$. What is the linear settling time required for 0.1 percent accuracy with?



Chapter 6 Figure 23

$$C_{\text{gs1}} = (2/3) \times 90 \times 0.4 \times 8.5 \text{ fF}/\mu\text{m}^2 = 0.21 \text{ pF}$$

The capacitance seen looking into the inverting input of the opamp is one-half this value since the gate-source capacitances of the two input devices are in series. Thus, the parasitic capacitance, C_p , is 0.11 pF. Therefore, the effective load capacitance is given by $C_L = 5 + 5 + \frac{5(5 + 0.11)}{5 + 5 + 0.11} = 12.53 \text{ pF}$

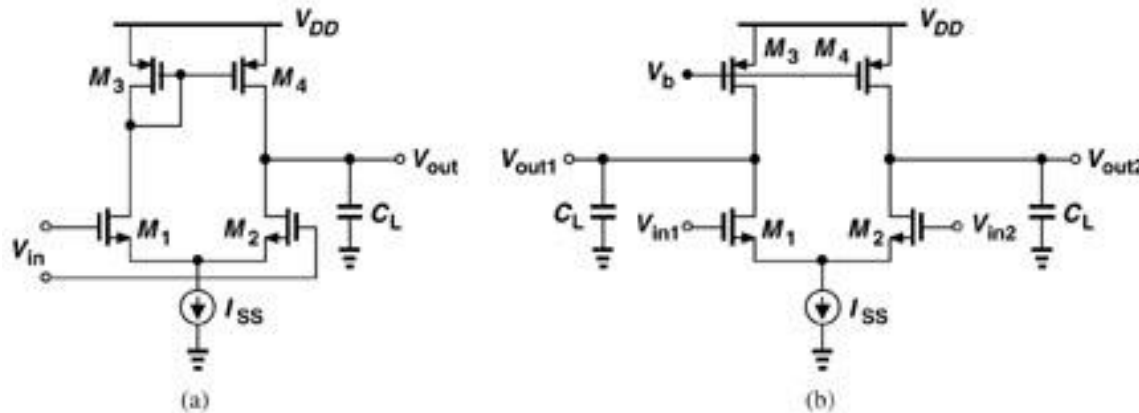
$$\omega_{\text{ta}} = \frac{Kg_{m1}}{C_L} = \frac{2 \times 2 \text{ mA/V}}{12.53 \text{ pF}} = 3.19 \times 10^8 \text{ rad/s} \quad \beta = \frac{5}{5 + 0.11 + 5} = 0.49$$

$$\tau = \frac{1}{\beta\omega_{\text{ta}}} = 6.4 \text{ ns}$$

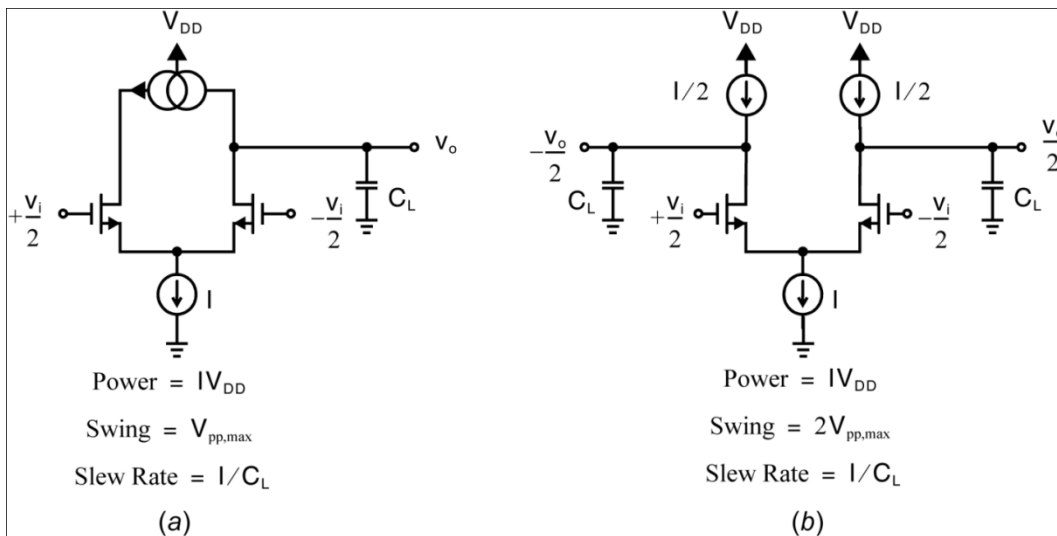
Finally, for 0.1 percent accuracy, we need a linear settling time of 7τ or 45 ns.

6.7 Fully differential amplifiers

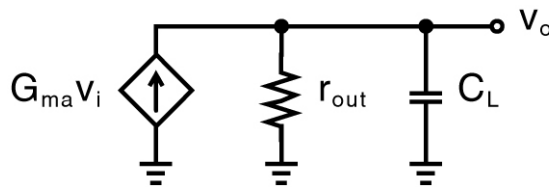
The main difference between single-ended amplifiers and fully-differential versions is that a current mirror load is replaced by two matched current sources in the later. Notice the power dissipation and slew rate is the same.



However, the voltage swing in fully-differential version is twice that of the single-ended version, because they use the differential voltage at two circuit nodes instead of one.



The small signal performance of a fully differential amplifier is in many way equivalent to that of a single-ended amplifier with similar power consumption. Fig. 6.25 illustrates the point for single-stage amplifiers. Assuming that the circuit's input stage is in both cases a differential pair under the same dc bias, and each half of the fully differential output has an output and load impedance similar to that of the single-ended output, the circuits have similar small-signal gain and bandwidth.

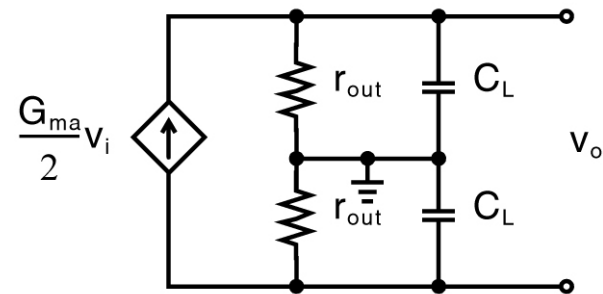


$$\text{dc gain: } G_{\text{ma}} r_{\text{out}}$$

$$\omega_{-3\text{dB}} = 1/(r_{\text{out}} C_L)$$

$$\omega_{\text{ta}} = G_{\text{ma}}/C_L$$

(a)



$$\text{dc gain: } \frac{G_{\text{ma}}}{2} 2r_{\text{out}} = G_{\text{ma}} r_{\text{out}}$$

$$\omega_{-3\text{dB}} = 1/(r_{\text{out}} C_L)$$

$$\omega_{\text{ta}} = G_{\text{ma}}/C_L$$

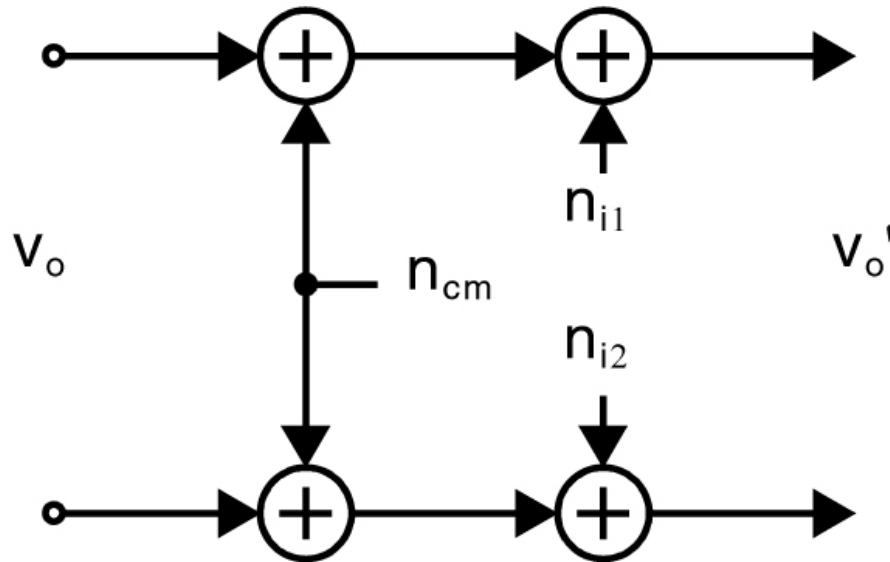
(b)

Why Fully differential amplifiers?

One of the main driving forces behind the use of fully differential amplifiers is to help reject common-mode noise. The common-mode noise, n_{cm} , appears identically on both half signals and is therefore cancelled when the difference between them is taken.

Many noise sources, such as power supply noise, bias voltage noise and switches noise act as common mode noise and can therefore be well rejected in fully-differential amplifiers.

n_{i1} and n_{i2} in the figure represent random noise sources added to the two outputs, and the overall signal-to-noise ratio is still better than the single-ended version.

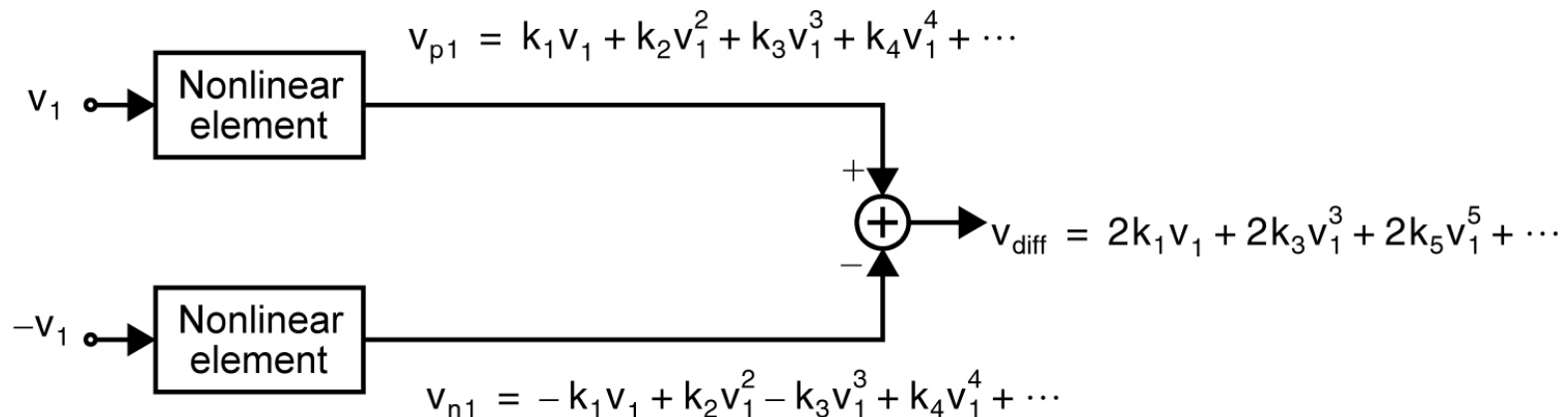


Why Fully differential amplifiers?

Fully –differential amplifiers have another benefit that if each output is distorted symmetrically around the common-mode voltage, the differential signal will have only odd-order distortion, which are often much smaller.

With the above mentioned advantages, most modern analog circuits are realized using fully differential structures.

One major drawback of using fully-differential OpAmp is that common-mode feedback circuit (CMFB to be discussed later) must be added to establish the common-mode output voltage. Another minor overhead is that in practice fully-differential OpAmp may need some additional power consumption due to CMFB and to producing the two outputs.



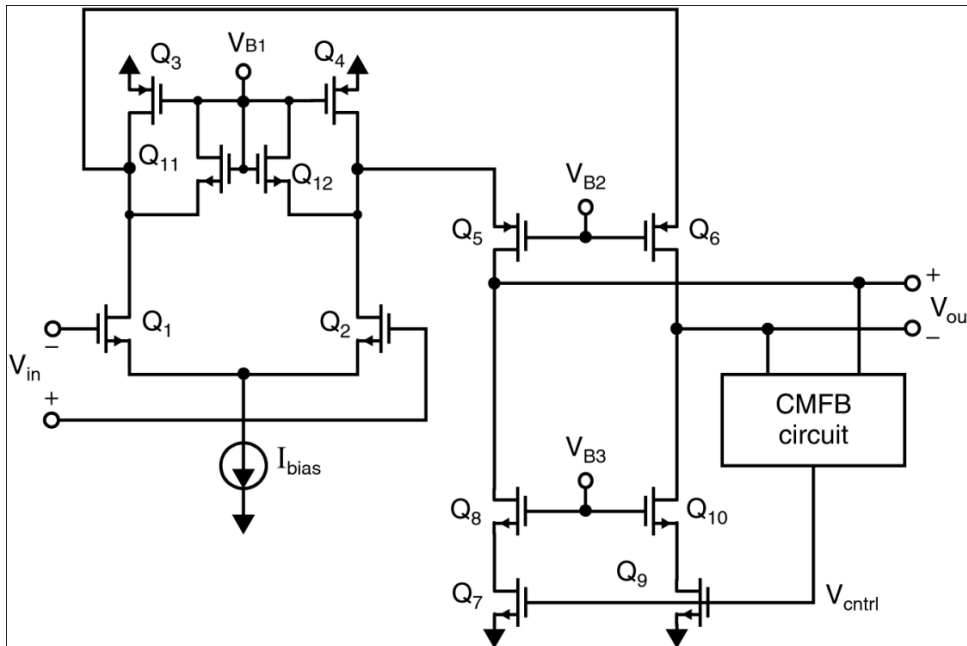
Chapter 6 Figure 27

6.7.1 Fully differential folded-cascode OpAmp

Compared to the singled-ended version, the n-channel current mirror has been replaced by two cascode current sources of Q7/8 and Q9/10. Also, a CMFB circuit is introduced. The gate voltage V_{cntrl} is the output of the CMFB.

Note that when OpAmp is slewing the maximum current for negative slew rate is limited by the bias current of Q7 or Q9 (as there is no current mirror like the singled-ended one). So, fully-differential FC is usually designed with bias current in the output stage equal to the bias currents in the input transistors.

Note that each signal path now consists of only one node in addition to the output nodes, which is the drain nodes of Q1/2. These nodes are responsible for the second pole.



Chapter 6 Figure 28

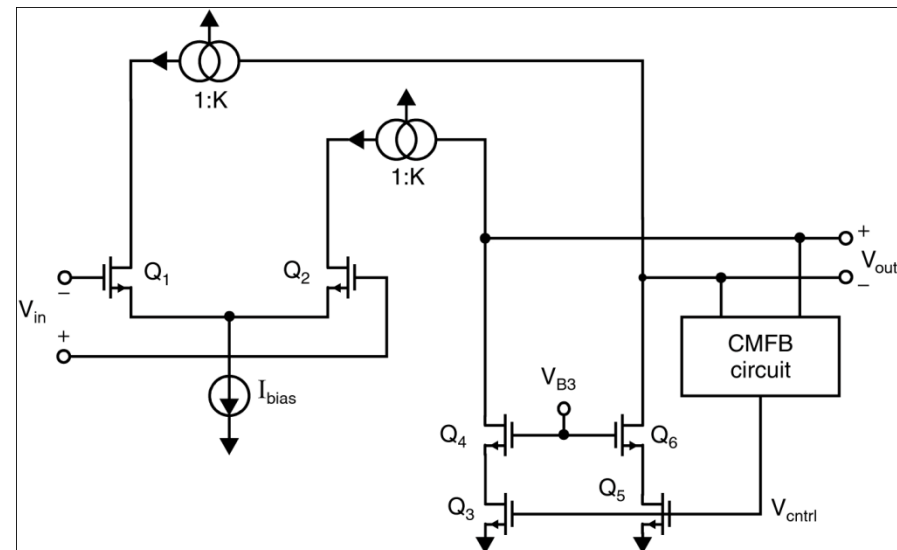
When load capacitance is relatively small so it is important to push the second pole away, then one can consider using pMOS for Q1/2 and nMOS for Q5/6, as the impedance at the drain of Q1/2 would be larger that way, resulting in smaller time constants. However, the tradeoff is DC gain may be smaller.

6.7.2 Alternative fully differential OpAmps

The previous singled-ended current mirror OpAmp can be converted to a fully-differential one as below.

Similarly, the complementary design using pMOS at input stage is possible. Which one to use depends on whether the load capacitance or second pole are limiting the bandwidth and whether DC gain or bandwidth is more important. (in the former case, then nMOS input is preferred.)

For a general-purpose amplifier, this design with large pMOS transistors, a current gain of $K=2$ and wide-wing enhanced output-impedance cascode mirrors and current sources may be a good choice compared to other designs.



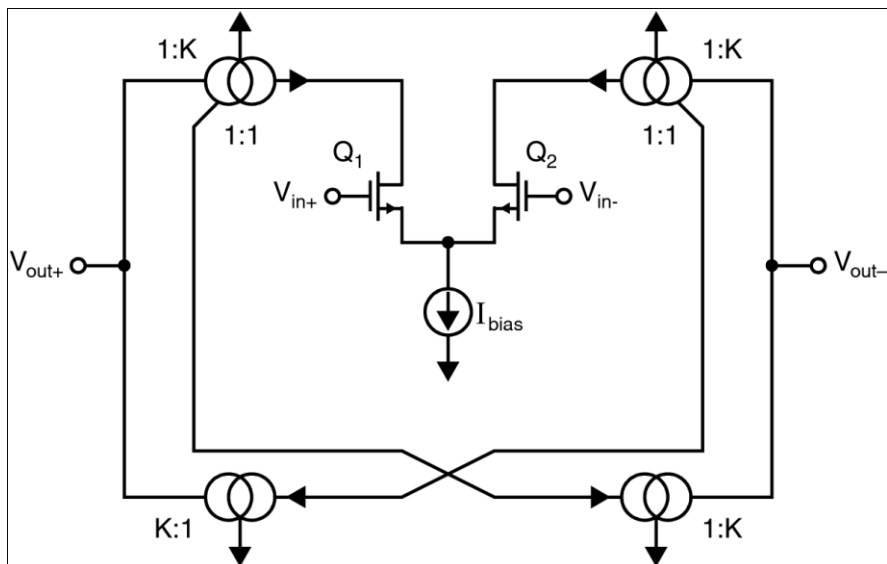
Slew rate $KI_B/2$ in each output

Larger slew rate

In the revised circuit, the current mirrors at the top have been replaced by current mirrors having two outputs. The first output has a gain of K and goes to the output of the OpAmp as before. The second output has a gain of one and goes to a new current mirror that has a current gain of K , where it is mirrored the second time and then goes to the opposite output.

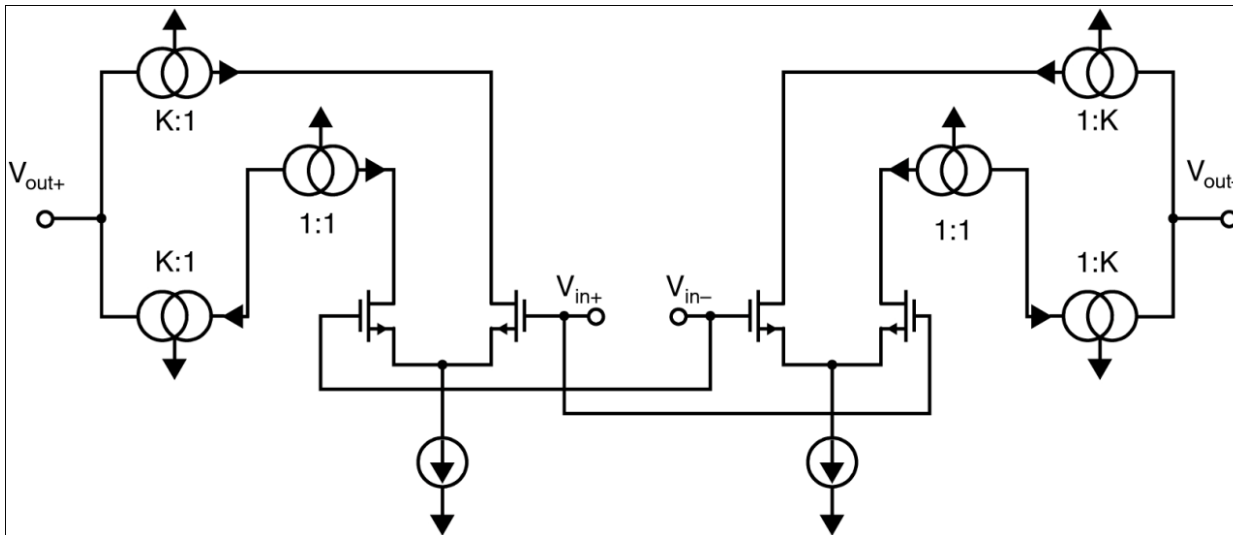
In this OpAmp, when slewing (suppose a very large input voltage), then the current going to V_{out+} is $K I_{bias}$, whereas the current sunk from V_{out-} is also $K I_{bias}$.

This OpAmp has an improved slew rate at the expense of slower small-signal response due to addition of extra current mirrors. But it may be worthwhile in some applications.



Another alternative design to have bi-direction driving capability is to use two singled-ended output OpAmps with their inputs connected in parallel and each of their output being one output side of the fully-differential version.

The disadvantage is the additional current mirrors and complexity. (note in the figure, the CMFB loop is not shown).

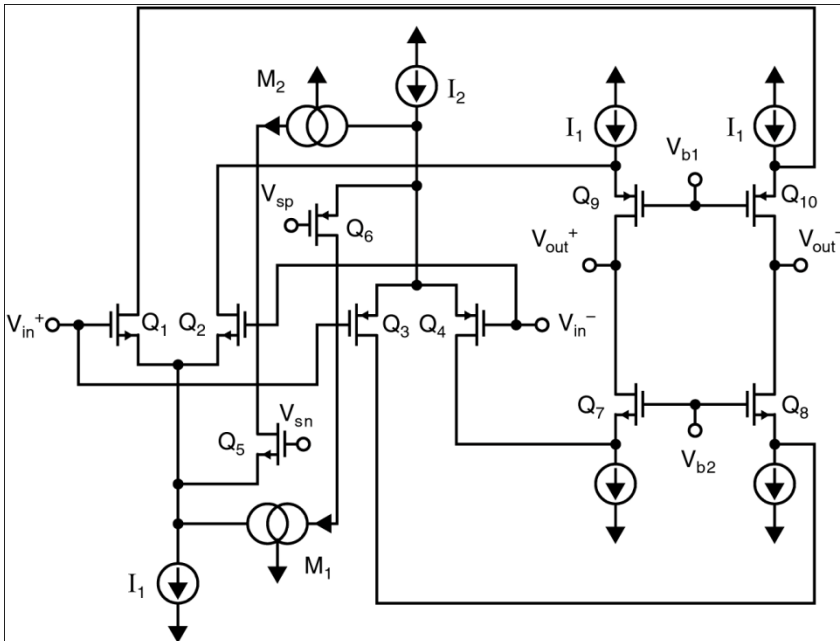


Chapter 6 Figure 31

6.7.3 Low supply voltage OpAmps

Low supply voltage complicates the OpAmp design. For the folded-cascode OpAmp, the input common-mode voltage must be large than $V_{gs1} + V_{eff}$ in order to keep the tail current source device in active mode (a typical value is 0.95V which is difficult for 1.2 power supply).

The low-voltage design shown below (CMFB circuit is not shown) makes use of both nMOS and pMOS in the two differential input pairs. When the input common-mode voltage range is close to one of the power supply voltages, one of input differential pairs turns off while the other one remains active. To keep the OpAmp gain relatively constant, the bias currents of the still-active pair is dynamically increased.



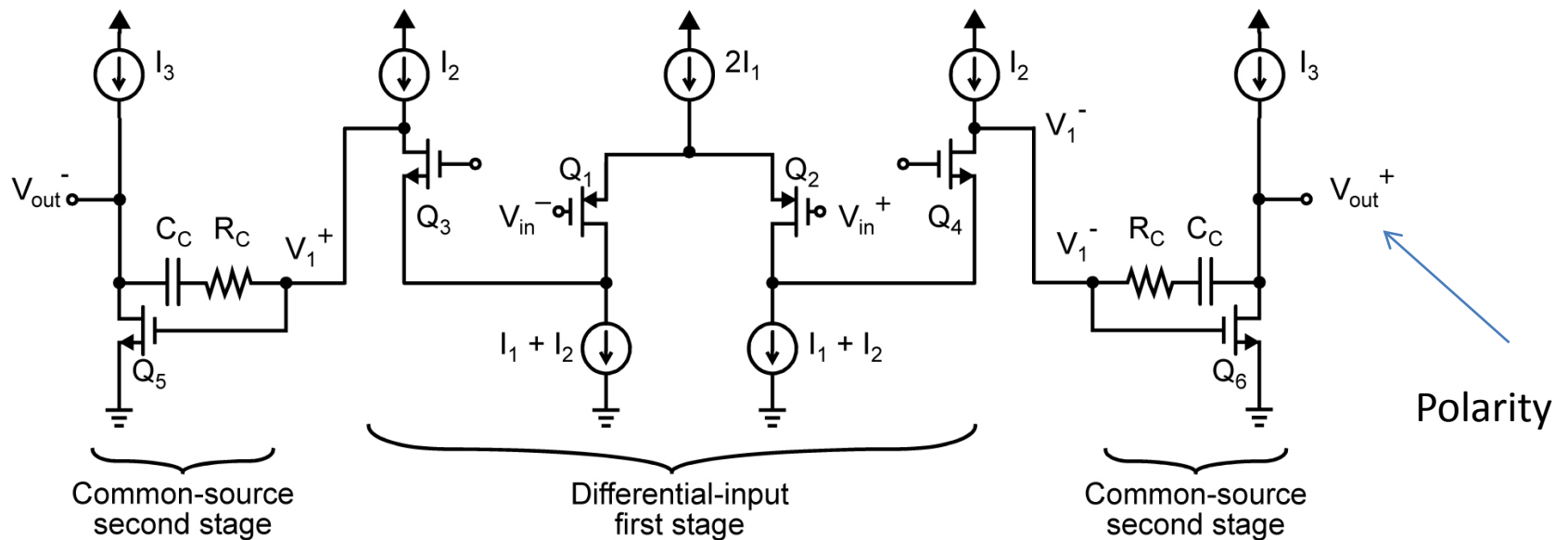
For example, when input common-mode voltage is close to V_{dd} , Q3/4 turns off and Q6 conduct all of I_2 , which go through a current mirror M1 so that the bias current of I_1 is increased.

Be careful about the input and output polarity!

Low supply voltage OpAmps

Another challenge of low supply voltage designs is that the signal output swing is very small, especially for the single-stage folded-cascode OpAmp (referring to the OpAmp in Fig 6.28, it can be shown that the signal swing is as small as 0.3V if $V_{\text{eff}}=0.2\text{V}$ for $V_{\text{dd}}=1.2\text{V}$).

One possible design to alleviate that problem is an enhanced two-stage OpAmp with a folded-cascode first stage and a common-source second stage. The first stage can provide high gain (small voltage swing for first stage output is not an issue) and the second stage can provide relatively large signal swing. (note CMFB is not shown and also the lead compensation is used.)



Chapter 6 Figure 33

6.8 Common-mode feedback circuits

To understand the need for CMFB, let us begin with a simple realization of a differential amplifier [Fig. 9.30(a)]. In some applications, we short the inputs and outputs for part of the operation [Fig. 9.30(b)], providing *differential* negative feedback. The input and output common-mode levels in this case are quite well-defined, equal to $V_{DD} - I_{SS}R_D/2$.

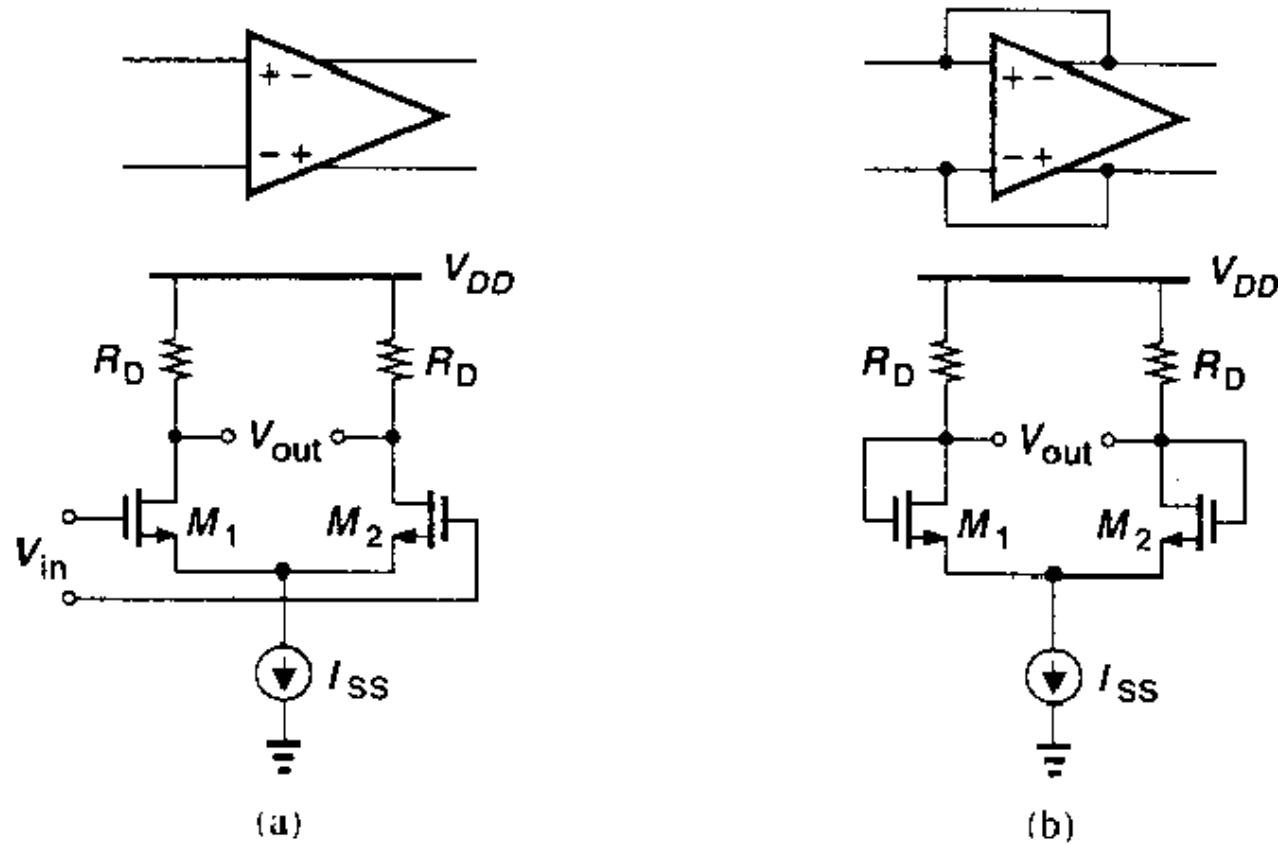


Figure 9.30 (a) Simple differential pair, (b) circuit with inputs shorted to outputs.

6.8 Common-mode feedback circuits

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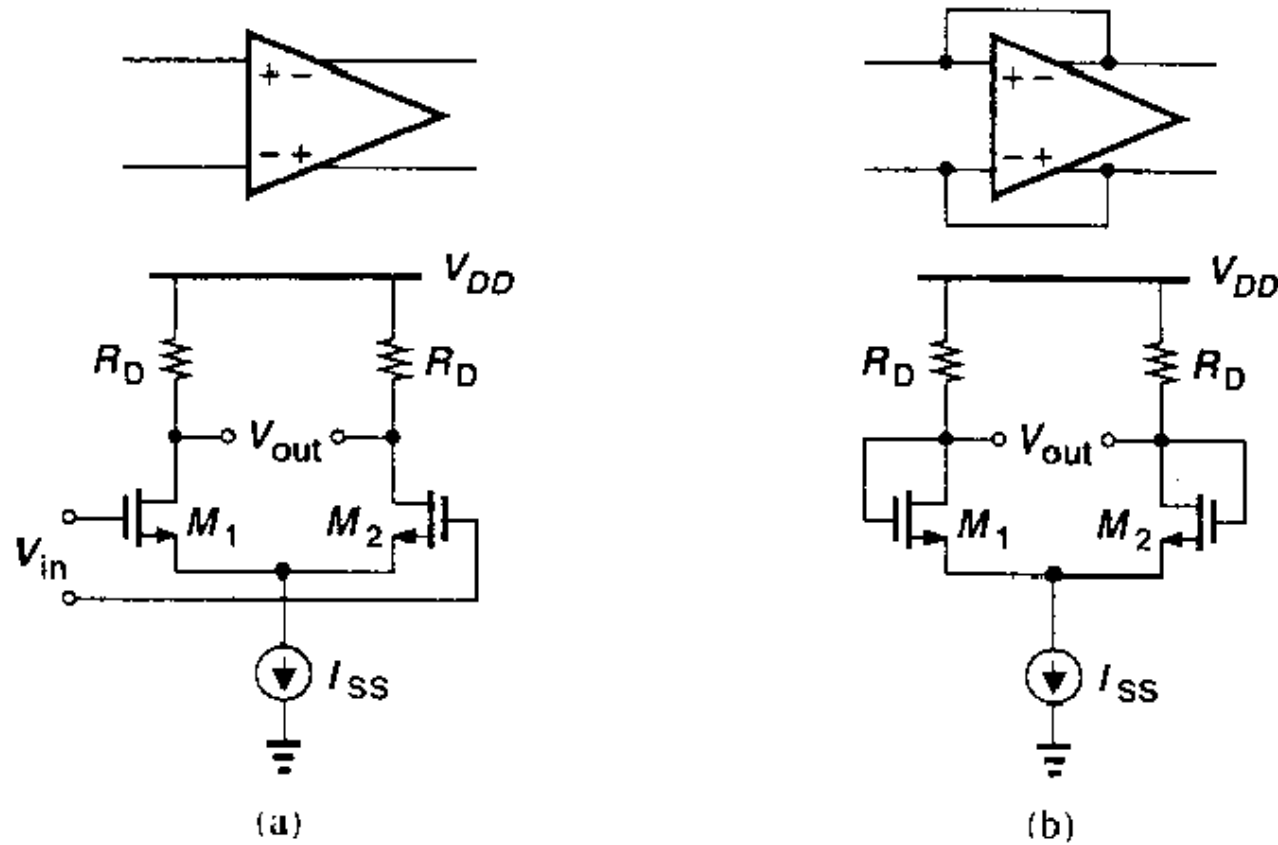


Figure 9.30 (a) Simple differential pair, (b) circuit with inputs shorted to outputs.

6.8 Common-mode feedback circuits

Now suppose the load resistors are replaced by PMOS current sources so as to increase the differential voltage gain [Fig. 9.31(a)]. What is the common-mode level at nodes X and Y ? Since each of the input transistors carries a current of $I_{SS}/2$, the CM level depends on how close I_{D3} and I_{D4} are to this value. In practice, as exemplified by Fig. 9.31(b), mismatches in the PMOS and NMOS current mirrors defining I_{SS} and $I_{D3,4}$ create a finite error between $I_{D3,4}$ and $I_{SS}/2$. Suppose, for example, that the drain currents of M_3 and M_4 in the saturation region are slightly greater than $I_{SS}/2$. As a result, to satisfy Kirchhoff current law at nodes X and Y , both M_3 and M_4 must enter the triode region so that their drain currents fall to $I_{SS}/2$. Conversely, if $I_{D3,4} < I_{SS}/2$, then both V_X and V_Y must drop so that M_5 enters the triode region, thereby producing only $2I_{D3,4}$.

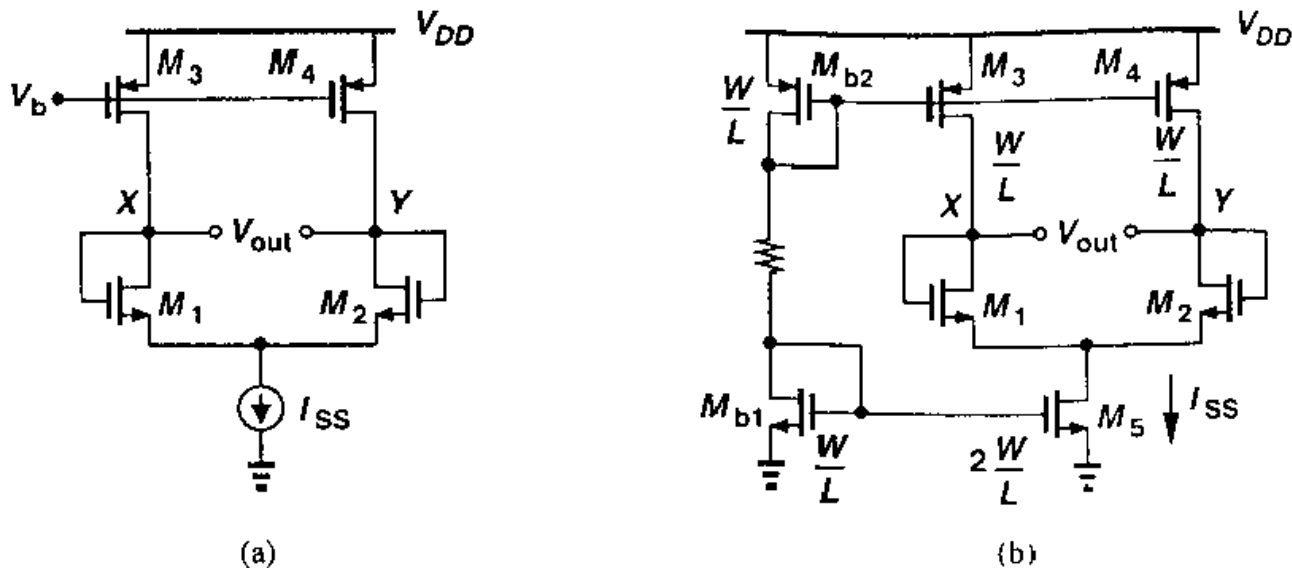


Figure 9.31 (a) High-gain differential pair with inputs shorted to outputs. (b) effect of current mismatches.

6.8 Common-mode feedback circuits

The above difficulties fundamentally arise because in high-gain amplifiers, we wish a p -type current source to balance an n -type current source. As illustrated in Fig. 9.32, the difference between I_P and I_N must flow through the intrinsic output impedance of the amplifier, creating an output voltage change of $(I_P - I_N)(R_P \parallel R_N)$. Since the current error depends on mismatches and $R_P \parallel R_N$ is quite high, the voltage error may be large, thus driving the p -type or n -type current source into the triode region. As a general rule, if the output CM level cannot be determined by “visual inspection” and requires calculations based on device properties, then it is poorly defined. This is the case in Fig. 9.31 but not in Fig. 9.30. We emphasize that differential feedback cannot define the CM level.

The foregoing study implies that in high-gain amplifiers, the output CM level is quite sensitive to device properties and mismatches and it cannot be stabilized by means of *differential* feedback. Thus, a common-mode feedback network must be added to sense the CM level of the two outputs and accordingly adjust one of the bias currents in the amplifier.

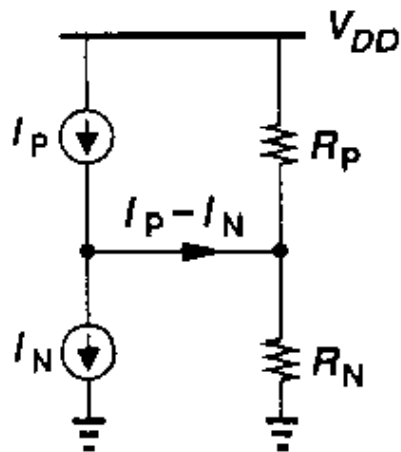


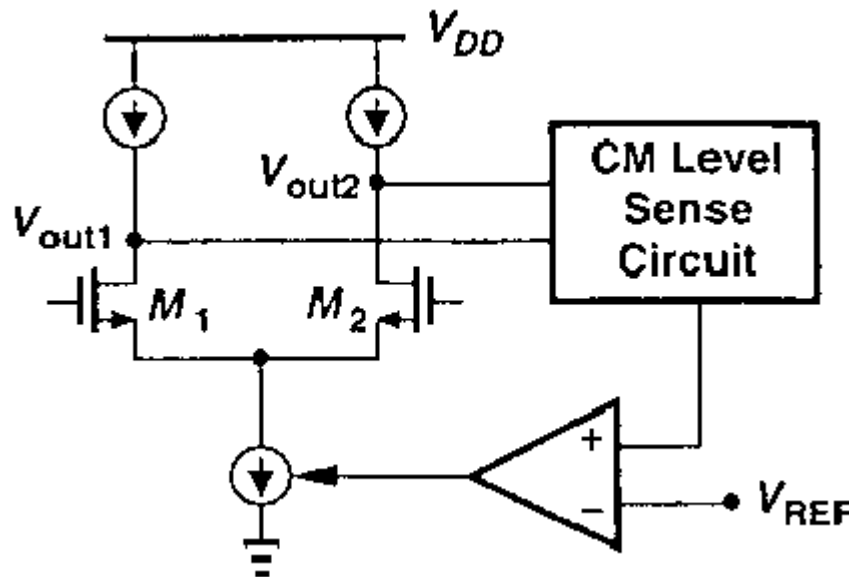
Figure 9.32 Simplified model of high-gain amplifier.

6.8 Common-mode feedback circuits

Typically, a CMFB circuit should have three operations:

1. Sense the common-mode voltage level of the differential output;
2. Compare the common-mode voltage to a reference voltage (the desired voltage);
3. Return the error to the amplifier's bias network to adjust the current and eventually the output voltage.

The following circuit illustrates the idea.



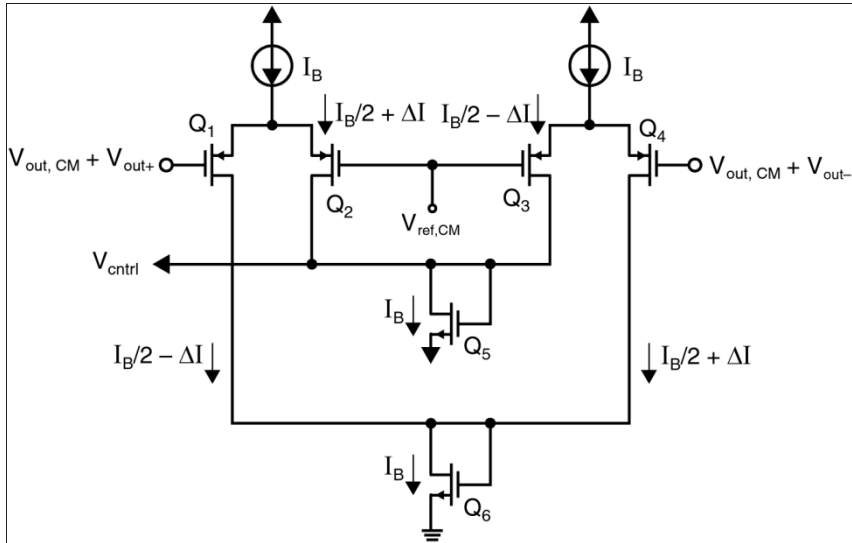
CMFB circuit design may well be one of the most difficult part of the OpAmp design.

6.8 Common-mode feedback circuits

There are two typical approaches to designing CMFB circuits—a continuous-time approach and a switched-capacitor approach. The former approach is often the limiting factor on maximizing the signal swings, and, if nonlinear, may actually introduce common-mode signals. The latter approach is typically only used in switched-capacitor circuits, since in continuous-time applications it introduces clock-feedthrough glitches.

The one shown below is a continuous one. To illustrate, assume CM output voltage, $V_{out,CM}$, equal to reference voltage $V_{ref,CM}$, and that v_{out+} is equal in magnitude but opposite in sign to V_{out-} . Also, assume the two differential pairs Q1/2 and Q3/4 have infinite CMRR (i.e. their output depend only on their differential voltage).

Since two pairs have the same differential voltages, current in Q1 is equal to current in Q3 and that in Q2 equal to Q4. Denoting the current in Q2 as $I_{D2} = I_B/2 + \Delta I$, and current in Q3 is $I_{D3} = (I_B/2) - \Delta I$, and the current in Q5 is $I_{D5} = I_{D2} + I_{D3} = (I_B/2 + \Delta I) + ((I_B/2) - \Delta I) = I_B$



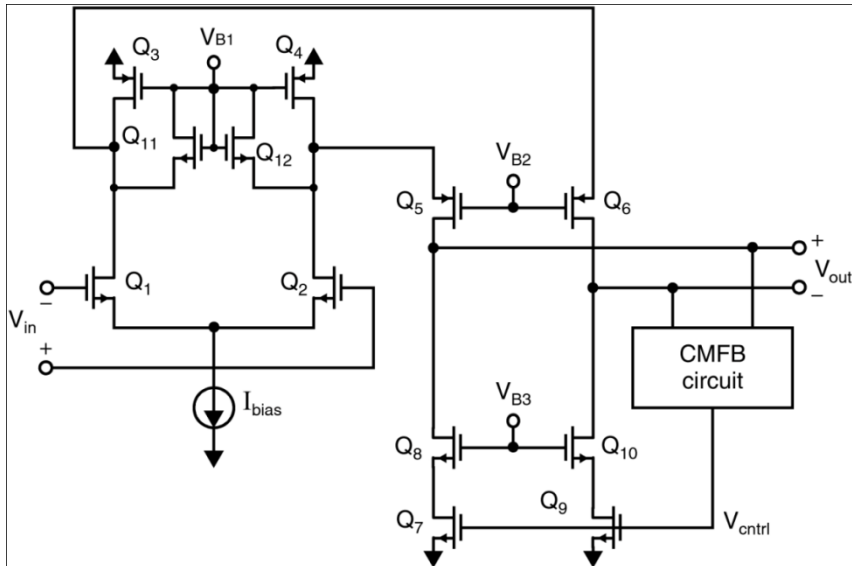
In the nominal case, when $V_{out,CM}=V_{ref,CM}$, then there will no voltage change for V_{cntrl} , which then stays constant.

If $V_{out,CM} > V_{ref,CM}$, then the differential voltage across Q1/2 increases while that for Q3/4 decreases, so the current in Q2 and Q3 will be larger than before, which increases the voltage V_{cntrl} .

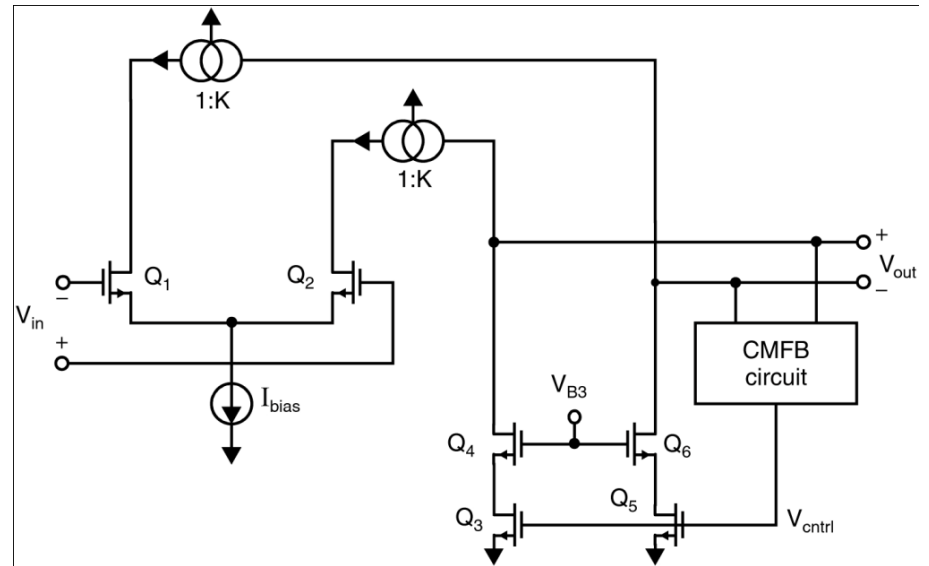
Now this voltage V_{cntrl} can be the bias voltage that sets the current levels in the nMOS current sources at the output of the OpAmp (see below), which will bring down the common-mode output voltage, $V_{\text{out,CM}}$ to decrease toward the nominal $V_{\text{ref,CM}}$.

So, as long as the common-mode loop gain is large enough, and the differential signals are not so large as to cause either differential pair $Q_1/2$ or $Q_3/4$ to turn off, $V_{\text{out,CM}}$ can be kept very close to $V_{\text{ref,CM}}$. The later requires that we maximize the V_{eff} for these transistors.

Finally, the I_B should be high output impedance cascode current sources to ensure good CMRR.



Chapter 6 Figure 28

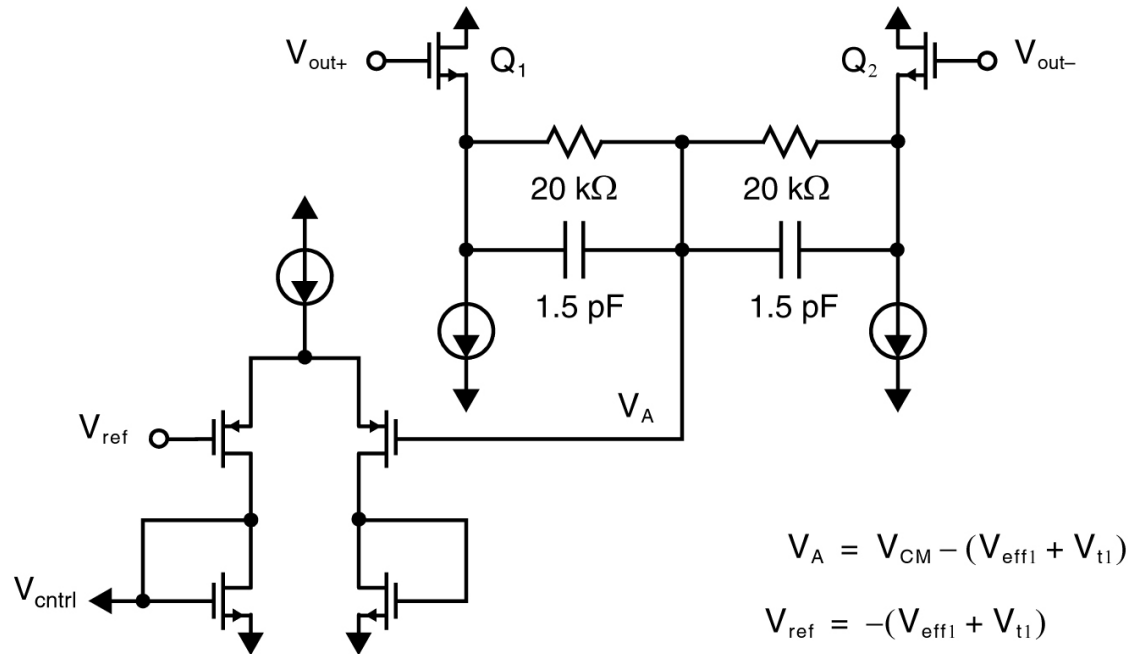


Chapter 6 Figure 29

Another CMFB

This circuit generates the senses the common-mode voltage of the output signals (minus a DC level shift) at node V_A . This voltage is then compared to a reference voltage, V_{ref} , using a separate amplifier.

One limitation is that the voltage drop across Q1/2 may severely limits the differential signals that can be processed, which is important in lower supply voltage applications.



Chapter 6 Figure 36

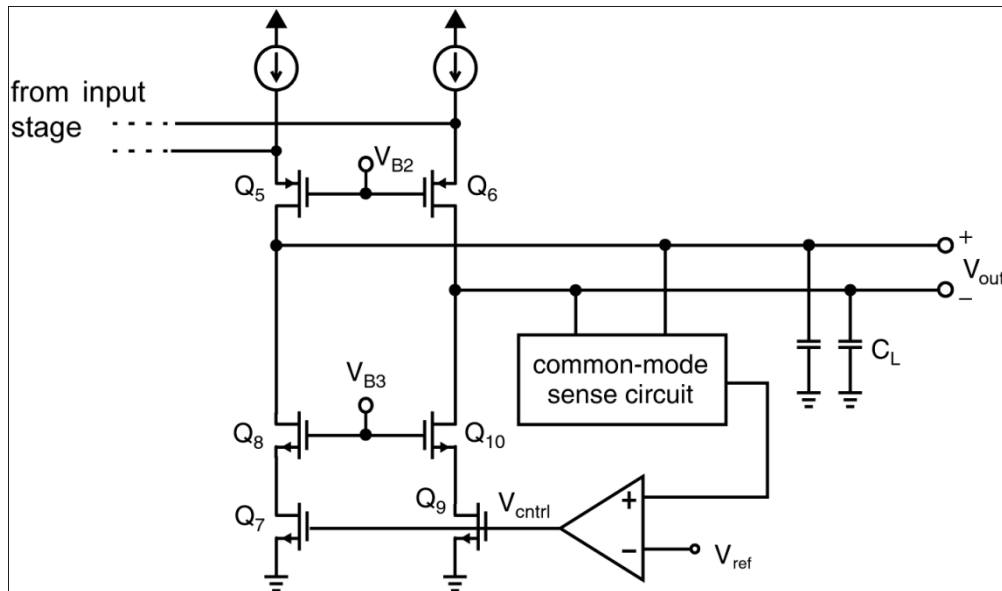
Design considerations of CMFB loop

One important design consideration is that CMFB is part of the negative feedback loop, and therefore must be well compensated if needed, otherwise the injection of common-mode signal can cause output ringing and even unstable. Thus, phase margin (by breaking at V_{cntrl} to find loop gain from Chapter 5) and step response (by giving V_{ref} a step input) of the common-mode loop should be checked.

Often, the common-mode loop is stabilized using the same capacitors used to compensate the differential loop (for example by connecting two compensation or load capacitors from outputs to ground).

Also, it is important to maximize the speed of CMFB loop by having as few nodes in the design as possible (to prevent high frequency common-mode noise). For this reason, the CFMB output is usually used to control current sources in the output stage of the OpAmp. For the same reason, the CM output of each stage in a multi-stage amplifier is individually compensated (for example the on in Fig 6.33.).

This is an active research area.

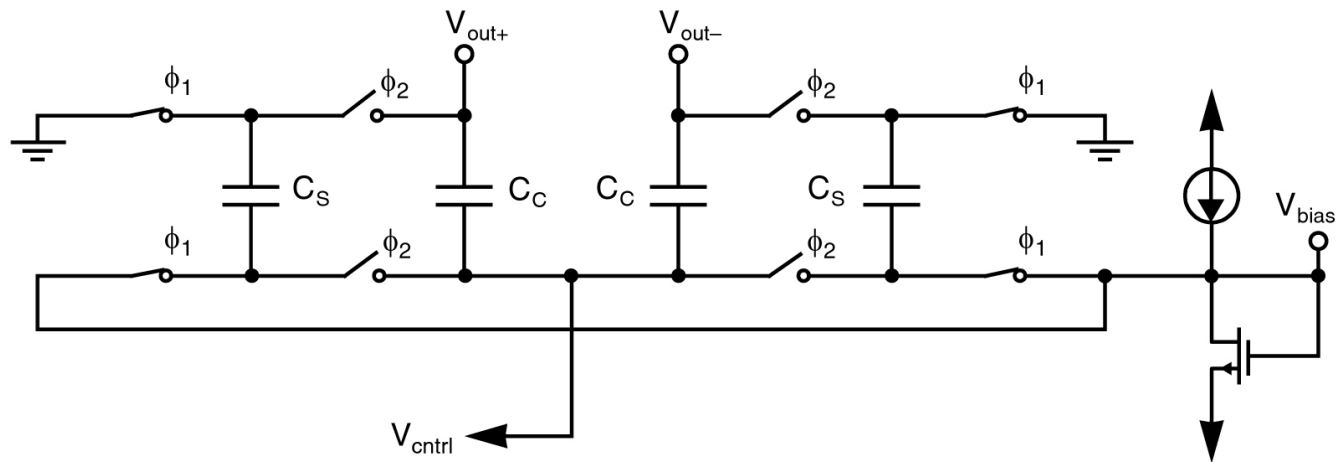


Chapter 6 Figure 37

Switch-capacitor CMFB circuit

In this approach, Capacitors C_c generates the $V_{out,CM}$, which is then used to create control voltages V_{cntrl} . The bias voltage V_{bias} is designed to be equal to the difference between the desired $V_{ref,CM}$ and the desired V_{cntrl} used for OpAmp current sources.

This CMFB circuit is mostly used in switched-capacitor circuits since they allow a larger output signal swing.



Chapter 6 Figure 38