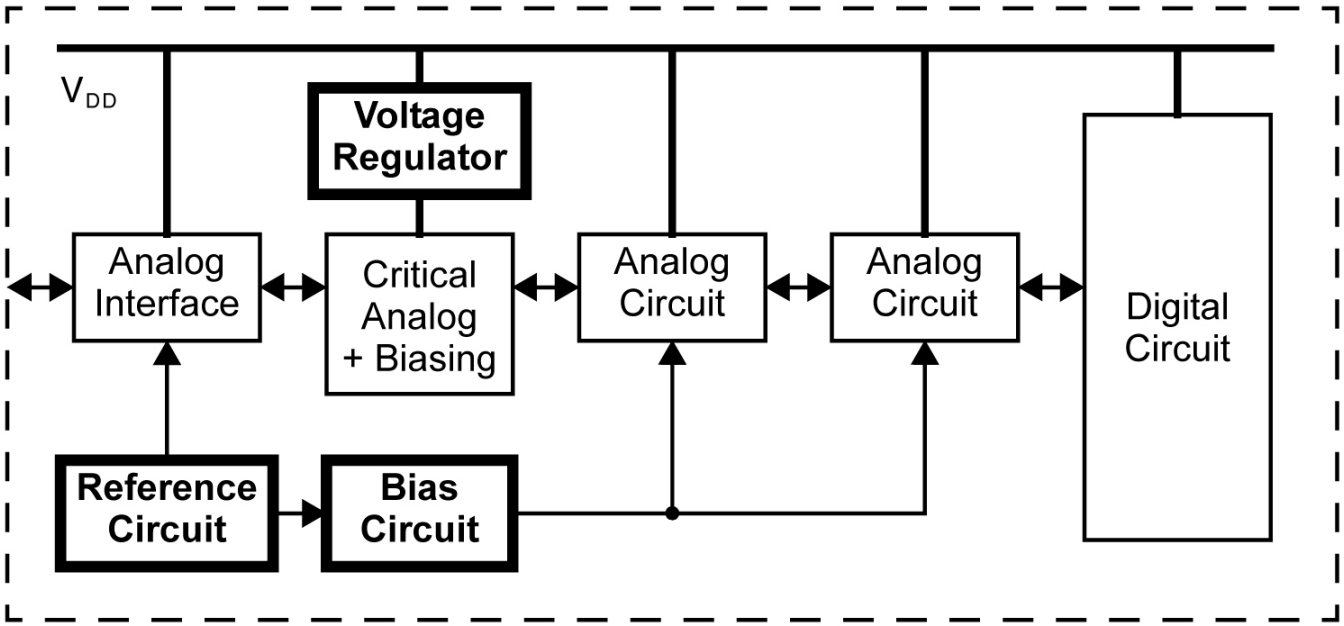
Biasing, References and Regulators

Chapter 7

7.1 Analog IC biasing

Although often ignored during the course of first-pass analog design, a critical factor in determining a circuit's overall performance is the quality of DC voltage and current sources.

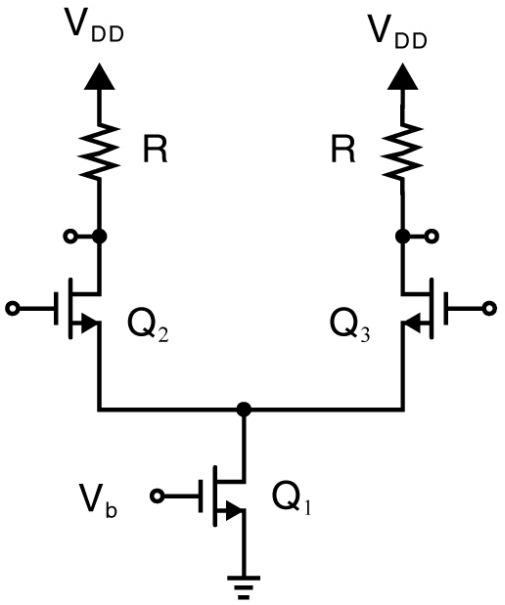
In an analog integrated circuit, many subcircuits work together to generate all of the various dc voltages and currents. These include bias circuits, reference circuits, and regulators. A *bias* circuit generates the dc voltages required to keep transistors near some desired operating point; of course, as transistor parameters change, either from chip to chip or with changes in temperature, so must the bias voltages. A *reference* circuit generates a voltage and/or current of a known fixed absolute value (for example, one volt). Finally, a *regulator* circuit improves the quality of a dc voltage or current, usually decreasing the noise. Fig. 7.1 shows how these circuits may work together to support the analog circuits on a large mixed analog–digital chip.



Chapter 7 Figure 01

7.1.1 Biasing circuits

Generally, the objective of a bias circuit is to ensure that the dc operating points of the transistors in an analog circuit remain within a desired range. Unlike a reference circuit, this means that the dc outputs of a bias circuit may adjust to process and temperature variations. Several approaches may be taken towards biasing. One is to ensure that circuits are biased to permit constant voltage swings; another is to ensure that constant currents are maintained; yet another is to try to ensure constant gain is maintained. These are illustrated in the following example.



Chapter 7 Figure 02

Consider the simple NMOS differential pair in Fig. 7.2 biased, nominally, with $V_{eff,1} = 200$ mV and $V_{tn} = 450$ mV. With a 10% decrease in both $\mu_n C_{ox}$ and R, and a 10% increase in V_{tn}, how must V_b change to ensure: a) a constant drain current in the matched differential pair devices $Q_{2,3}$; b) a constant voltage drop across the resistors R; c) a constant gain.

(a) $I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_b - V_{tn})^2$. $V_b = V_{tn} + V_{eff,1} = 1.1(450\text{ mV}) + (200\text{ mV})/(\sqrt{0.9}) = 706\text{ mV}$.

(b) $V_b = 1.1(450\text{ mV}) + (200\text{ mV})/(0.9\sqrt{0.9}) = 729\text{ mV}$.

(c) The small-signal gain of the differential pair is $g_{m2}R$ where it may be shown that

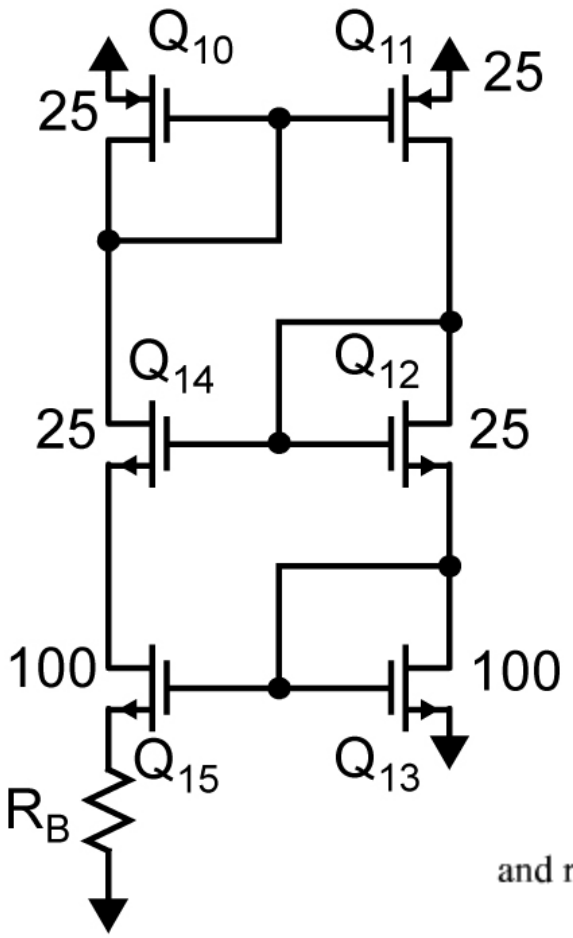
$$g_{m2} \alpha \mu_n C_{ox}(V_b - V_{tn})$$

$$V_b = 1.1(450\text{ mV}) + (200\text{ mV})/(0.9 \cdot 0.9) = 742\text{ mV}$$

Example 7.1 illustrates the challenge of designing a good bias circuit which must somehow monitor multiple device parameters and automatically adjust multiple analog voltages to achieve a desired effect.

7.2.1 basic constant-g_m circuit

As transconductance is probably the most important parameters in an analog amplifier, it needs to be stabilized. An approach proposed by Steininger may be used to stabilize g_m independent of power supply, process and temperature variations.



Chapter 7 Figure 06

$(W/L)_{10} = (W/L)_{11}$. This equality results in both sides of the circuit having the same current due to the current-mirror pair Q_{10}, Q_{11}. As a result, we also must have $I_{D15} = I_{D13}$. Now, around the loop consisting of Q_{13}, Q_{15}, and R_B, we have

$$V_{GS13} = V_{GS15} + I_{D15}R_B \tag{7.3}$$

$$V_{eff13} = V_{eff15} + I_{D15}R_B$$

$$\sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}} = \sqrt{\frac{2I_{D15}}{\mu_n C_{ox}(W/L)_{15}}} + I_{D15}R_B$$

and since $I_{D13} = I_{D15}$, we can also write

$$\sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}} = \sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{15}}} + I_{D13}R_B$$

Rearranging, we obtain $$\frac{2}{\sqrt{2\mu_n C_{ox}(W/L)_{13}I_{D13}}}\left[1 - \sqrt{\frac{W/L_{13}}{W/L_{15}}}\right] = R_B$$

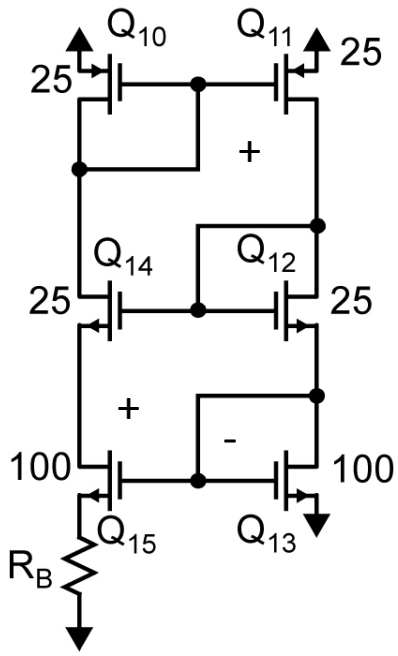
and recalling that $g_{m13} = \sqrt{2\mu_n C_{ox}(W/L)_{13}I_{D13}}$ results in the important relationship

$$g_{m13} = \frac{2\left[1 - \sqrt{\dfrac{(W/L)_{13}}{(W/L)_{15}}}\right]}{R_B}$$

7.2.1 basic constant-gm circuit

Thus, the transconductance of Q_{13} is determined by R_B and geometric ratios only, independent of power-supply voltages, process parameters, temperature, or any other parameters with large variability. For the special case of $(W/L)_{15} = 4(W/L)_{13}$, we have simply

$$g_{m13} = \frac{1}{R_B} \tag{7.9}$$



Chapter 7 Figure 06

Not only is g_{m13} stabilized, but all other transconductances are also stabilized since all transistor currents are derived from the same biasing network, and, therefore, the ratios of the currents are mainly dependent on geometry. For example, for all n-channel transistors,

$$g_{mi} = \sqrt{\frac{(W/L)_i I_{Di}}{(W/L)_{13} I_{D13}}} \times g_{m13} \tag{7.10}$$

and for all p -channel transistors

$$g_{mi} = \sqrt{\frac{\mu_p}{\mu_n} \frac{(W/L)_i I_{Di}}{(W/L)_{13} I_{D13}}} \times g_{m13}$$

May vary from chip-to-chip

Please note the positive feedback from common source Q11, to common source Q15. For stability, it requires R_B to be large enough so that Q15 has a gain much less than 1.0.

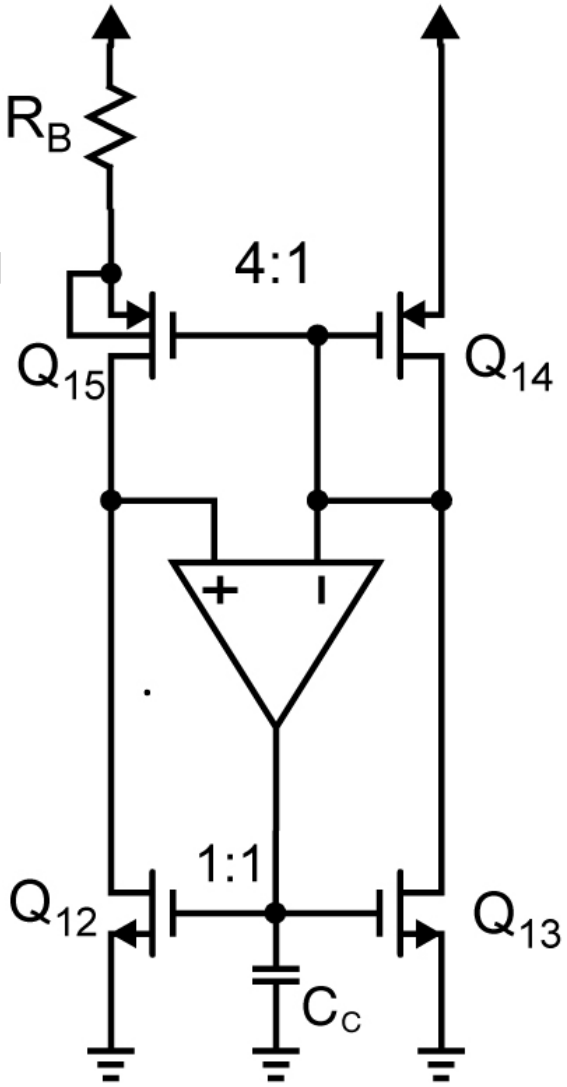
7.2.1 basic constant-g_m circuit

Body effect plays a role for Q15. Also, channel length modulation affects the circuit as well.

Both effects can be mitigated using a modified circuit. Here, Q14/15 become pMOS devices, and body of Q15 is connected to source to eliminate body effect. Furthermore, an amplifier is used to maintain equal voltages at the transistor drain terminals, reducing output impedance effects.

In addition to the positive feedback, now OpAmp and Q12/13 form a negative feedback, which may need to be stabilized by compensation capacitor Cc.

A fundamental limitation is that at high temperatures, the currents and V_{eff} increases to compensate carrier mobility degradation to keep g_m constant, and this may limit signal swing in lower supply voltages. Therefore, V_{eff} is not to be designed too large (0.2-0.25V at T=300k).



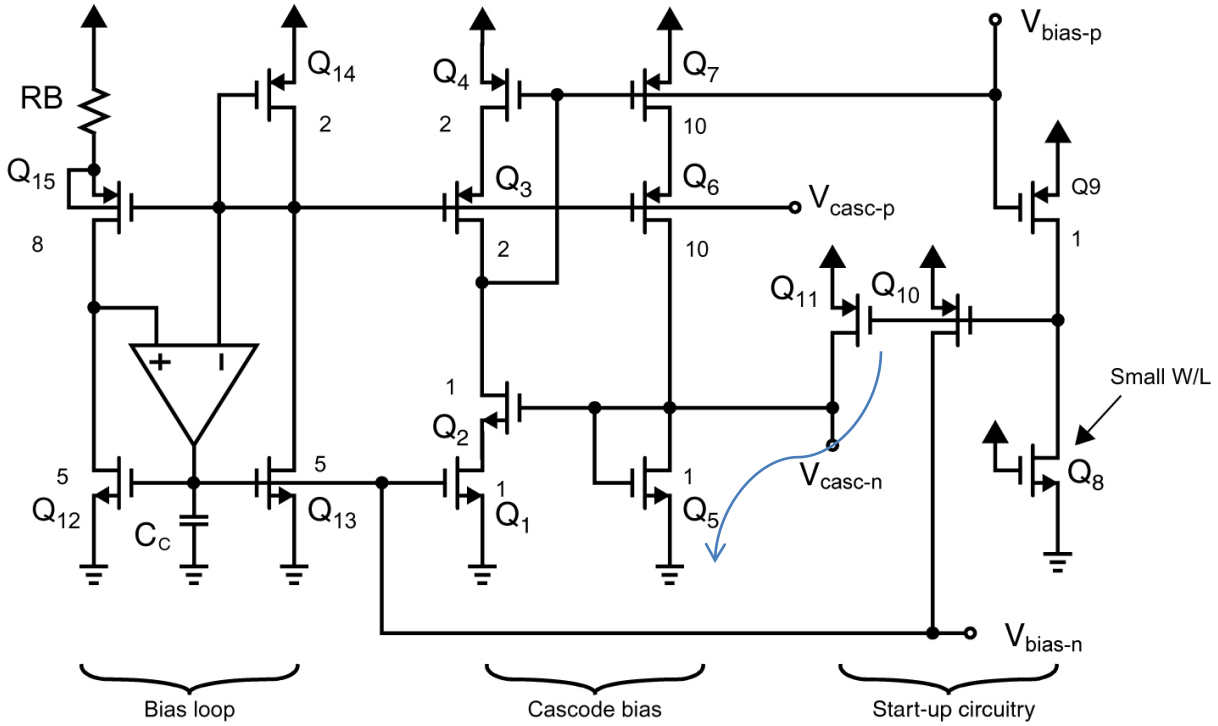
Chapter 7 Figure 07

7.2.2 Improved constant-g_m circuit

It is possible to have wide-swing current mirrors to the constant-g_m circuit to provide biasing voltages.

A constant-transconductance bias is provided by transistors Q_{12-15}, so that $g_{m14} = 1/R_B$

An example start-up circuit is also given to prevent all current going to 0. If that happens, Q9 is off, Q8 is always on, then gates of Q10/11 pulled low, which then injects currents to the bias loop, which start up the circuit. After that, Q9 on, pull gates of Q10/11 high, turning them off so they do not affect the circuit operation anymore.



Chapter 7 Figure 08

7.1.2 Reference circuits

Known absolute values of voltage or current are most useful at the interface between integrated circuits, or between an integrated circuit and some other discrete component.

A reference voltage or current may sometimes be derived from the supply voltage, but the supply is not always controlled with sufficient accuracy in which case a reference voltage or current must be produced by an integrated reference circuit.

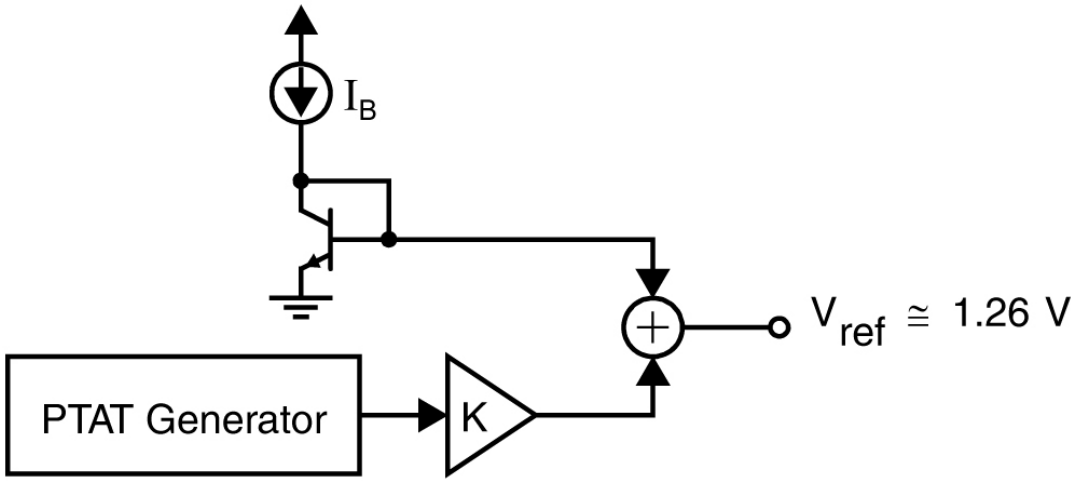
Unfortunately, although dimensionless quantities may be accurately controlled on integrated circuits (e.g., ratios of device sizes), there are very few dimensioned quantities that do not vary significantly from one integrated circuit to another, or with variations in temperature.

7.3 Establishing constant voltages/currents

An important analog building block is a voltage reference. Ideally, this block will supply a fixed DC voltage of known amplitude that does not change with temperature. This can be combined with an accurate resistance to provide a stable DC current.

The most popular approach is to cancel the negative temperature dependence of a PN junction with a positive temperature dependence from a PTAT (proportional to absolute temperature) circuit. PTAT is usually realized by amplifying the voltage difference of two forward-biased base-emitter (or Diode) junctions.

Voltage references realized this way is called “Bandgap” voltage references.



Chapter 7 Figure 09

7.3 Establishing constant voltages/currents

A forward-biased base-emitter junction of a bipolar transistor[3] has an I-V relationship given by

$$I_C = I_S e^{qV_{BE}/kT}$$

$$V_{BE} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\frac{T}{T_0} + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{J_C}{J_{C0}}\right) \qquad (7.14)$$

Here, V_{G0} is the bandgap voltage of silicon extrapolated to 0 K (approximately 1.206 V), k is Boltzmann's constant, and m is a temperature constant approximately equal to 2.3. Also, J_C and T are the collector current density and temperature, respectively, while the subscript 0 designates an appropriate quantity at a reference temperature, T_0. Specifically, J_{C0} is the collector current density at the reference temperature, T_0, whereas J_C is the collector current density at the true temperature, T. Also, V_{BE0} is the junction voltage at the reference temperature, T_0, whereas V_{BE} is the base-emitter junction voltage at the true temperature, T. Note that the junction current is related to the junction current density according to the relationship

$$I_C = A_E J_C \qquad (7.15)$$

where A_E is the effective area of the base-emitter junction.

For I_C constant, V_{BE} will have approximately a -2 mV/°K temperature dependence around room temperature. This negative temperature dependence is cancelled by a PTAT temperature dependence of the amplified difference of two base-emitter junctions biased at fixed but different current densities. Using (7.14), it is seen that if there are two base-emitter junctions biased at currents J_2 and J_1, then the difference in their junction voltages is given by

$$\Delta V_{BE} = V_2 - V_1 = \frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right) \qquad (7.16)$$

Example 7.3 (page 312)

Assume two transistors are biased at a current-density ratio of 10:1 at $T = 300$ K. What is the difference in their base-emitter voltages and what is its temperature dependence?

Solution

Using (7.16), we have

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{J_2}{J_1}\right) = \frac{1.38 \times 10^{-23}(300)}{1.602 \times 10^{-19}} \ln(10) = 59.5 \text{ mV} \tag{7.17}$$

Since this voltage is proportional to absolute temperature, after a 1 K temperature increase, the voltage difference will be

$$\Delta V_{BE} = 59.5 \text{ mV} \frac{301}{300} = 59.7 \text{ mV} \tag{7.18}$$

Thus, the voltage dependence is 59.5 mV/300 K or 0.198 mV/K. Since the temperature dependence of a single V_{BE} is −2 mV/K, if it is desired to cancel the temperature dependence of a single V_{BE}, then ΔV_{BE} should be amplified by about a factor of 10, as explained next.

Example 7.3 (page 312)

Junction currents are usually proportional to absolute temperature $\frac{J_i}{J_{i0}} = \frac{T}{T_0}$

Now, assume that the difference between two base-emitter voltages is multiplied by a factor of K and added to the base-emitter voltage of the junction with the larger current density.

$$V_{ref} = V_{BE2} + K\Delta V_{BE}$$
$$= V_{G0} + \frac{T}{T_0}(V_{BE0\text{-}2} - V_{G0}) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + K\frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right) \quad (7.20)$$

Equation (7.20) is the fundamental equation giving the relationship between the output voltage of a bandgap voltage reference and temperature. Here, $V_{BE0\text{-}2}$ is the base-emitter junction voltage of the second transistor at temperature T_0. If we want zero temperature dependence at a particular temperature, we can differentiate (7.20) with respect to temperature and set the derivative to zero at the desired reference temperature. From (7.20), we have

$$\frac{\partial V_{ref}}{\partial T} = \frac{1}{T_0}(V_{BE0\text{-}2} - V_{G0}) + K\frac{k}{q}\ln\left(\frac{J_2}{J_1}\right) + (m-1)\frac{k}{q}\left[\ln\left(\frac{T_0}{T}\right) - 1\right] \quad (7.21)$$

Setting (7.21) equal to zero at $T = T_0$, we see that for zero temperature dependence at the reference temperature,

$$V_{BE0\text{-}2} + K\frac{kT_0}{q}\ln\left(\frac{J_2}{J_1}\right) = V_{G0} + (m-1)\frac{kT_0}{q} \quad (7.22)$$

The left side of (7.22) is the output voltage V_{ref} at $T = T_0$ from (7.20). Thus for zero temperature dependence at $T = T_0$, we need

$$V_{ref\text{-}0} = V_{G0} + (m-1)\frac{kT_0}{q} \quad (7.23)$$

bandgap

For the special case of $T_0 = 300\ ^\circ K$ and $m = 2.3$, (7.23) implies that

$$V_{ref\text{-}0} = 1.24\ V \quad \text{for zero temperature dependence.} \quad (7.24)$$

Example 7.3 (page 312)

From (7.22), the required value for K is

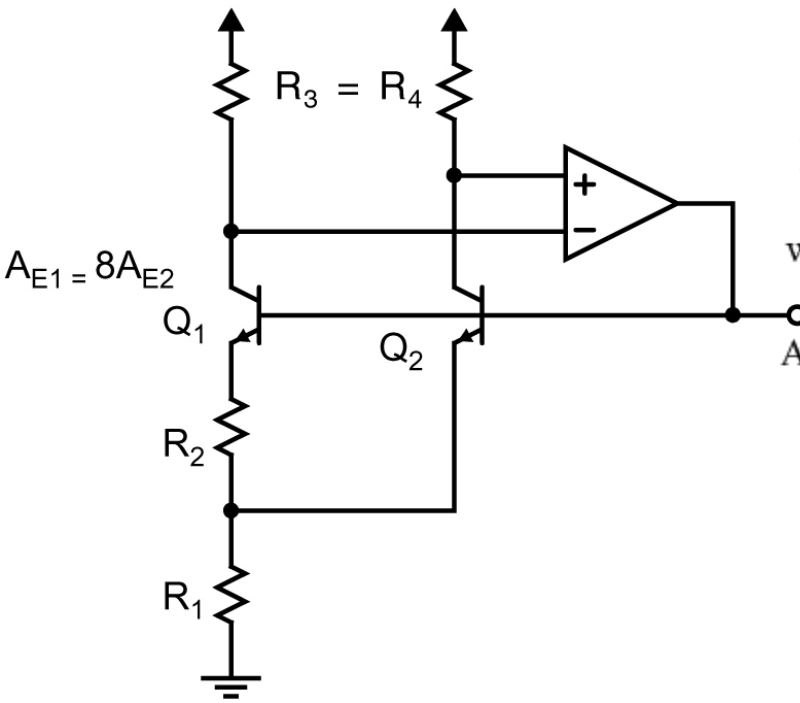
$$K = \frac{V_{G0} + (m-1)\frac{kT_0}{q} - V_{BE0\text{-}2}}{\frac{kT_0}{q}\ln\left(\frac{J_2}{J_1}\right)} = \frac{1.24 - V_{BE0\text{-}2}}{0.0258\ \ln\left(\frac{J_2}{J_1}\right)} \qquad \text{at } 300\ ^\circ\text{K}. \qquad (7.25)$$

7.3.2 Circuits for bandpap references

A voltage reference originally proposed in [Brokaw, 1974] has been the basis for many bipolar bandgap references. A simplified schematic of the circuit is shown in Fig. 7.10. The amplifier in the feedback loop keeps the collector voltages of Q_1 and Q_2 equal. Since $R_3 = R_4$, this guarantees that both transistors have the same collector currents and collector-emitter voltages. Also, notice that the emitter area of Q_1 has been taken eight times larger than the emitter area of Q_2. Therefore, Q_2 has eight times the current density of Q_1, resulting in

$$\frac{J_2}{J_1} = 8 \tag{7.30}$$

$$V_{ref} = V_{BE2} + V_{R1}$$



Chapter 7 Figure 10

$$V_{R1} = I_{R1}R_1 = 2I_{R2}R_1$$

$$I_{R2} = \frac{V_{R2}}{R_2} = \frac{V_{BE2} - V_{BE1}}{R_2} = \frac{\Delta V_{BE}}{R_2} \rightarrow V_{ref} = V_{BE2} + \frac{2R_1}{R_2}\Delta V_{BE}$$

which is of the form desired to realize a bandgap reference. $K = \frac{2R_1}{R_2}$

Assuming $V_{BE2\text{-}0} = 0.65$ V, from (7.25)

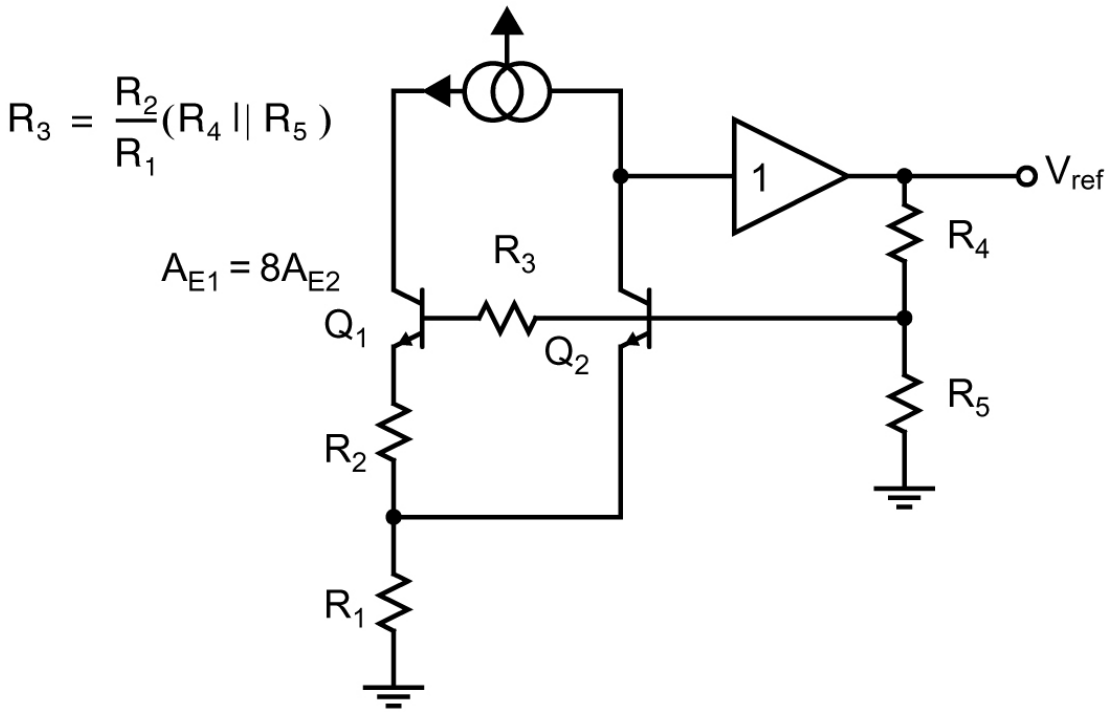
$$\frac{R_1}{R_2} = \frac{1}{2} \times \frac{1.24 - 0.65}{0.0258 \times \ln(8)} = 5.5$$

7.3.2 Bipolar bandgap references

In applications where it is desirable to have reference voltages larger than 1.24 V, a modified bandgap reference as shown in Fig. 7.11 can be used. It is not difficult to show that the output voltage is now given by

$$V_{ref\text{-}0} = \left(1 + \frac{R_4}{R_5}\right)\left[V_{G0} + (m-1)\frac{kT_0}{q}\right] \cong \left(1 + \frac{R_4}{R_5}\right)1.24\ \text{V} \qquad (7.38)$$

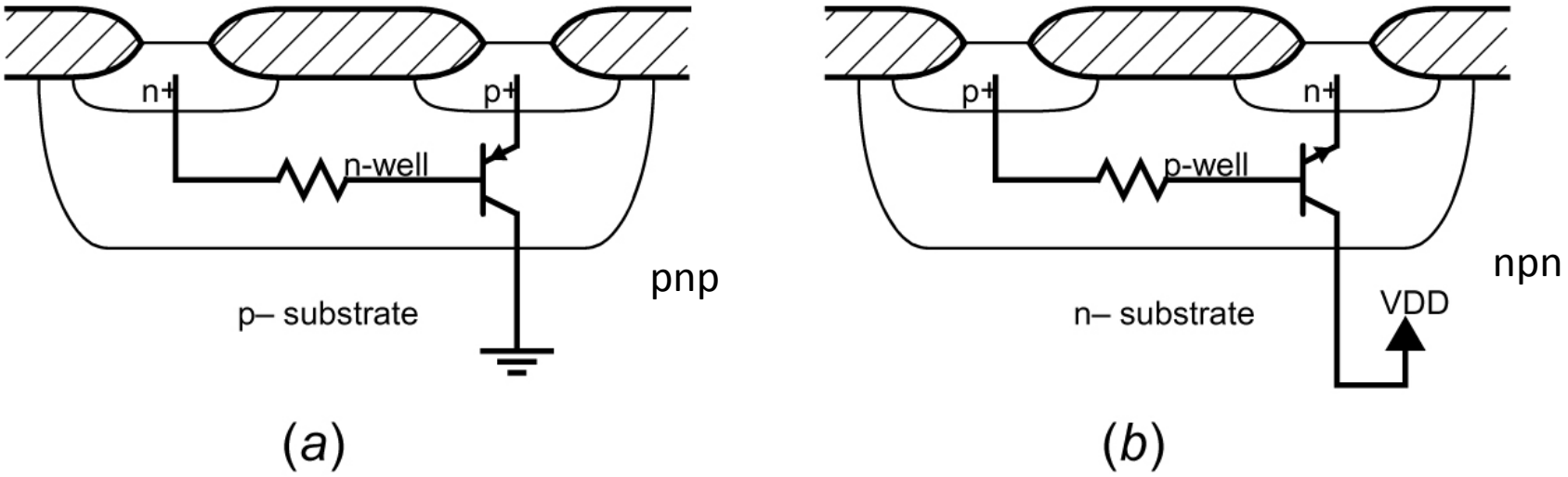
Resistor R_3 has been added to cancel the effects of the finite base currents going through R_4 and should be chosen according to the formula in the figure.



Chapter 7 Figure 11

CMOS bandgap references

The most popular method for realizing CMOS voltage references also makes use of a bandgap voltage reference despite the fact that *independent* bipolar transistors are not available. These CMOS circuits rely on using what are commonly called *well transistors*. These devices are vertical bipolar transistors that use wells as their bases and the substrate as their collectors. In an n-



Chapter 7 Figure 12

With respect to the n-well implementation of Fig. 7.13(*a*), we have

$$V_{ref} = V_{EB1} + V_{R1}$$

Also, assuming the opamp has large gain and that its input terminals are at the same voltage, then

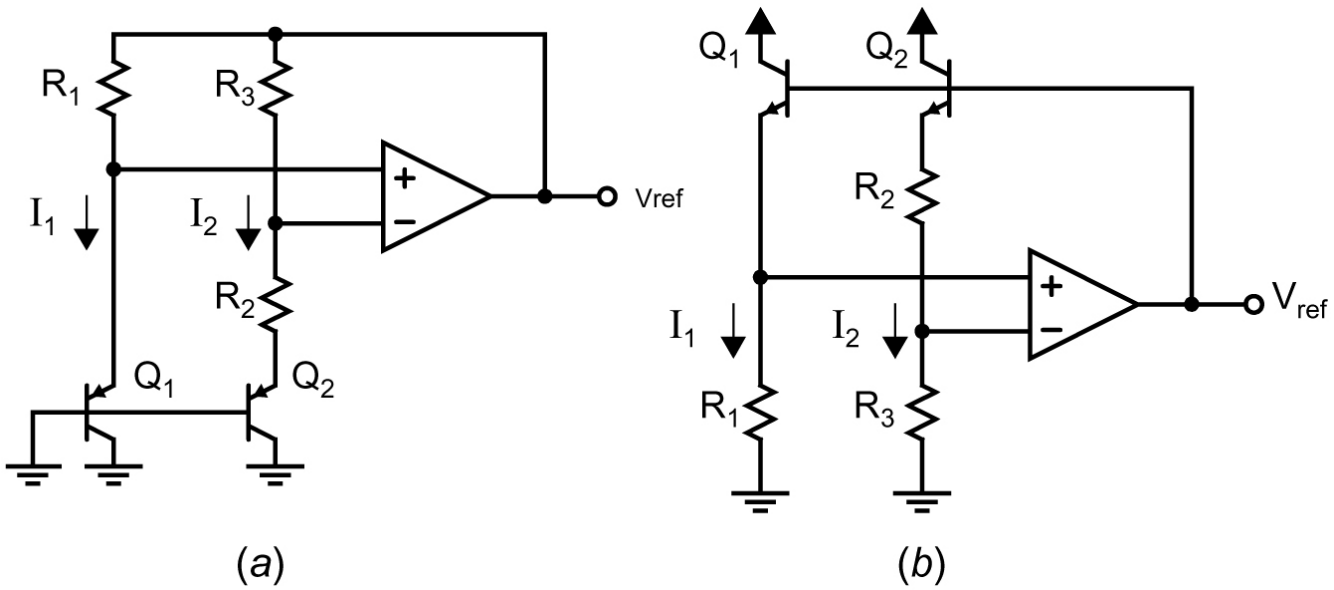
$$V_{R2} = V_{EB1} - V_{EB2} = \Delta V_{EB}$$

Now, since the current through R_3 is the same as the current through R_2, we have

$$V_{R3} = \frac{R_3}{R_2} V_{R2} = \frac{R_3}{R_2} \Delta V_{EB}$$

the voltage across R_1 equal to the voltage across R_3. $V_{ref} = V_{EB1} + \frac{R_3}{R_2} \Delta V_{EB} \longrightarrow K = \frac{R_3}{R_2}$

which is in the required form to realize a bandgap reference.

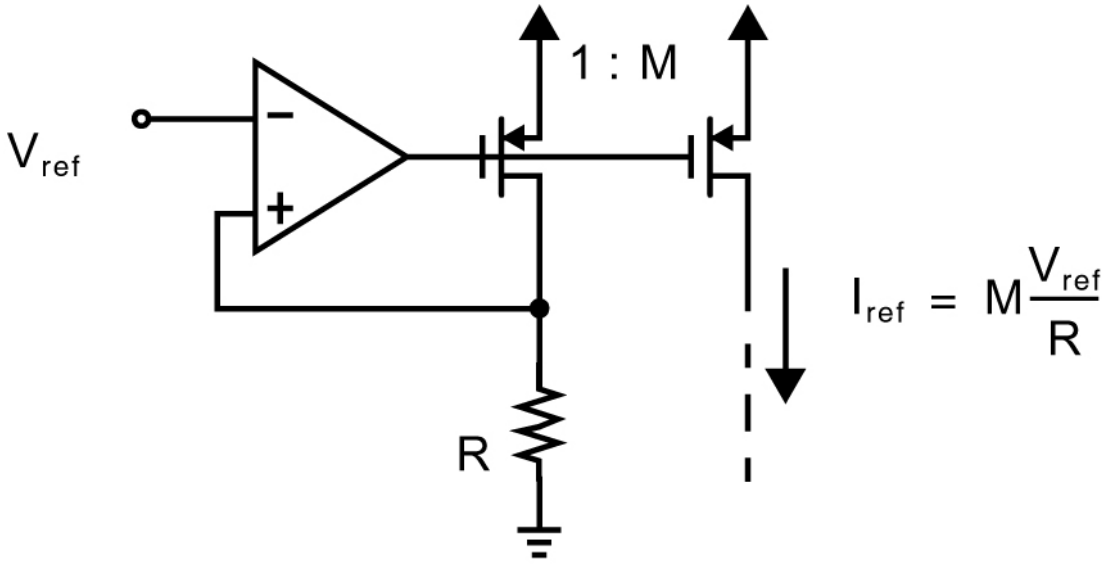


(*a*) (*b*)

Chapter 7 Figure 13

Once a bandgap voltage has been established, it can be used in combination with a resistor to provide a reference current. The basic approach is illustrated in Fig. 7.16. Feedback is used to generate the PMOS gate voltage that results in a voltage drop of precisely V_{ref} across a resistor R. This gate voltage can then be used to generate a scaled copy of the resulting current, $I_{ref} = MV_{ref}/R$.

If absolute current is needed, on-chip R needs to be trimmed and temperature-compensated. Off-chip R can be used as well.



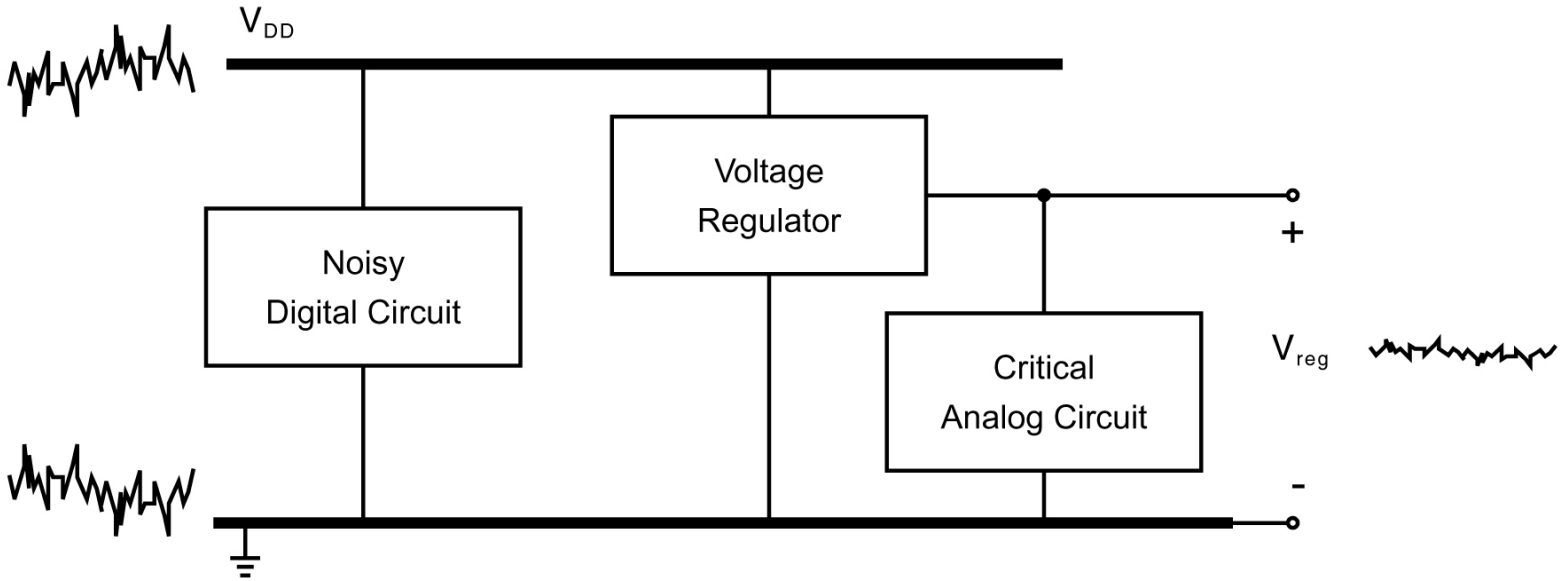
Chapter 7 Figure 16

7.1.3 Regulator circuits

A regulator's main purpose is to produce a voltage which has low noise and from which some current may be drawn. They are common when a critical analog circuit must operate from the same power supply voltage as other circuits. As other circuits or especially digital circuits introduce significant (called digital switching noise) to the common supply, a regulator can maintain a relatively quite supply for the critical circuit.

As digital circuits are major sources of power supply noise, regulators are common in today's mixed analog-digital IC.

The regulated voltage is generally lower than the regulator's supply voltage.

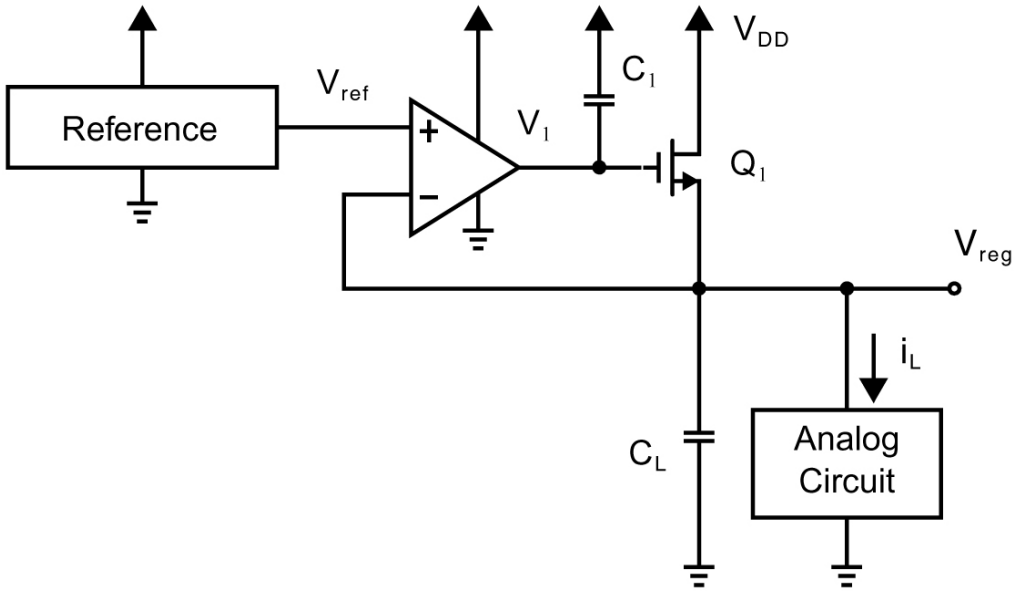


Chapter 7 Figure 05

7.4 Voltage regulation

A voltage regulator produces a low-noise dc voltage from which some current can be drawn. Its primary use is to provide a quiet supply voltage to an analog circuit, particularly in environments when a noisy supply voltage will otherwise limit performance.

A basic voltage regulator is shown in Fig. 7.17. It accepts as input a reference voltage, V_{ref}, and produces as output V_{reg}. It is essentially a unity-gain feedback buffer. The amplifier provides gain in the loop which ensures $V_{reg} \cong V_{ref}$ while Q_1, called the pass transistor, sources the load current. The reference input may be derived from a bandgap circuit, if it is to remain fixed over process and temperature variations. Variable-output regulators have a fixed reference voltage and incorporate a resistive voltage divider in the feedback loop which is adjusted to effect change in the output voltage.



Chapter 7 Figure 17

7.4.1 Specifications

Power Supply Rejection

A regulator's ability to maintain a quiet voltage at V_{reg} in the presence of noise on V_{DD} is measured by superimposing a small signal onto V_{DD} and measuring the resulting variations in V_{reg}. The ratio of the two small signals v_{dd} and v_{reg} is its power supply rejection ratio which is usually expressed in decibels and is frequency-dependent.

$$PSRR(\omega) = 20\log_{10}|v_{dd}/v_{reg}| \text{ dB} \tag{7.61}$$

Output Impedance

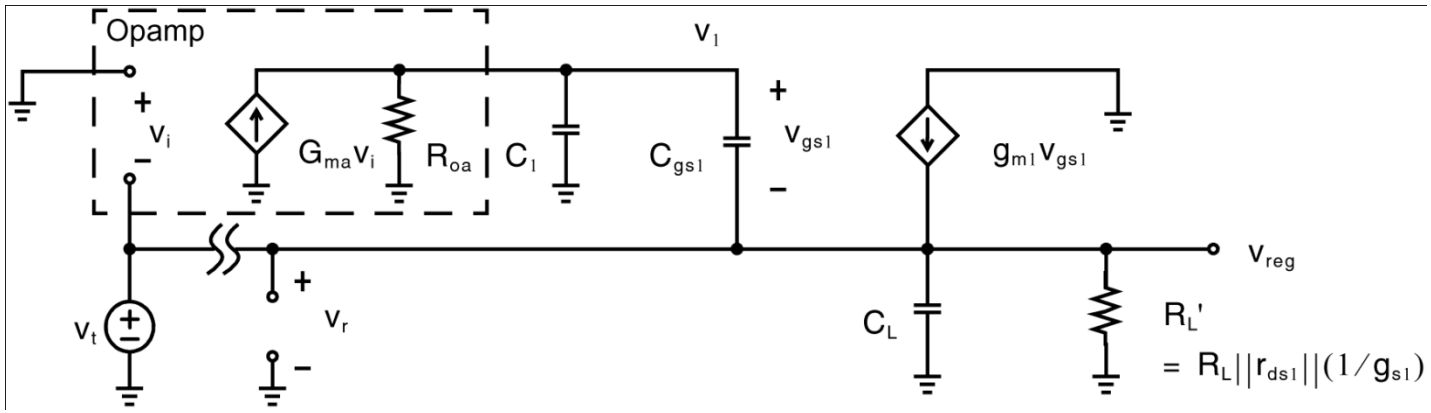
Variations in the current drawn by the regulator's load, i_L, will generally cause variations in V_{reg}. If the changes are small, they are related by the regulator's small-signal output impedance, Z_{out}. At high frequencies, this will be determined by the impedance of the load capacitance, $1/j\omega C_L$. At low frequencies, it is determined by the impedance of the pass transistor $1/g_{m,1}$ divided by the opamp gain.

Dropout Voltage

$V_{DD} - V_{reg}$, called the *dropout voltage*, V_{DO}. and to minimize V_{DO}.

If the opamp is operated under the same supply voltage as Q_1, and assuming the opamp output must be at least V_{eff} below V_{DD} to prevent some device there from entering triode, the dropout voltage is at least $2V_{eff} + V_{tn,1}$. This quantity is not too large if native NMOS devices (having $V_{tn} \approx 0$) are available. Alternatively, in some cases the opamp is operated from a higher supply voltage.

7.4.2 Feedback analysis



Chapter 7 Figure 18

Assuming a single-stage opamp with transconductance G_{ma} and output resistance R_{oa},

$$L(s) = \left(\frac{G_{ma}R_{oa}R_L'}{R_L' + 1/g_{m1}}\right)\frac{\left(1 + \frac{sC_{gs1}}{g_{m1}}\right)}{\left(1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}\right)}$$

$$\omega_0 = \sqrt{\frac{(1/R_{oa})(g_{m1} + 1/R_L')}{C_{gs1}C_L + C_1(C_{gs1} + C_L)}}$$

$$Q = \frac{\sqrt{(1/R_{oa})(g_{m1} + 1/R_L')[C_{gs1}C_L + C_1(C_{gs1} + C_L)]}}{C_L/R_{oa} + C_1(g_{m1} + 1/R_{oa}) + C_{gs1}/R_L'}$$

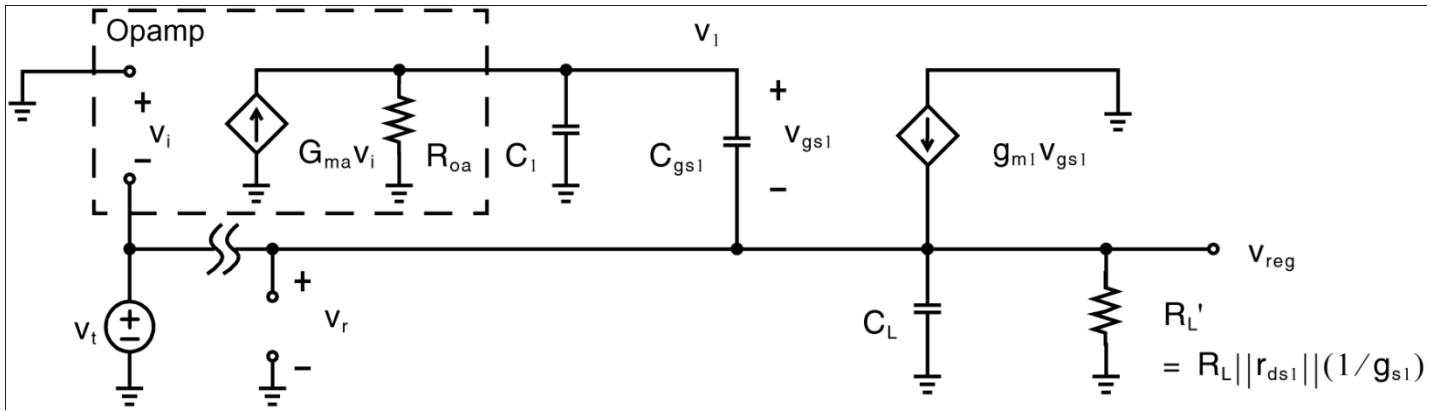
Assuming the loop is dominant-pole compensated, then $Q \ll 1$

$$-\omega_{p1} = -\omega_0 Q = -\frac{(1/R_{oa})(g_{m1} + 1/R_L')}{C_L/R_{oa} + C_1(g_{m1} + 1/R_{oa}) + C_{gs1}/R_L'}$$

$$-\omega_{p2} = -\frac{\omega_0}{Q} = -\frac{C_L/R_{oa} + C_1(g_{m1} + 1/R_{oa}) + C_{gs1}/R_L'}{C_{gs1}C_L + C_1(C_{gs1} + C_L)}$$

$$-\omega_z = -g_{m1}/C_{gs1}$$

7.4.2 Feedback analysis



Chapter 7 Figure 18

There are two different ways to compensate the loop. If C_1 is made large the dominant pole $\omega_{p1} \approx 1/R_{oa}C_1$

Alternatively, C_L can be made very large and R_{oa} decreased

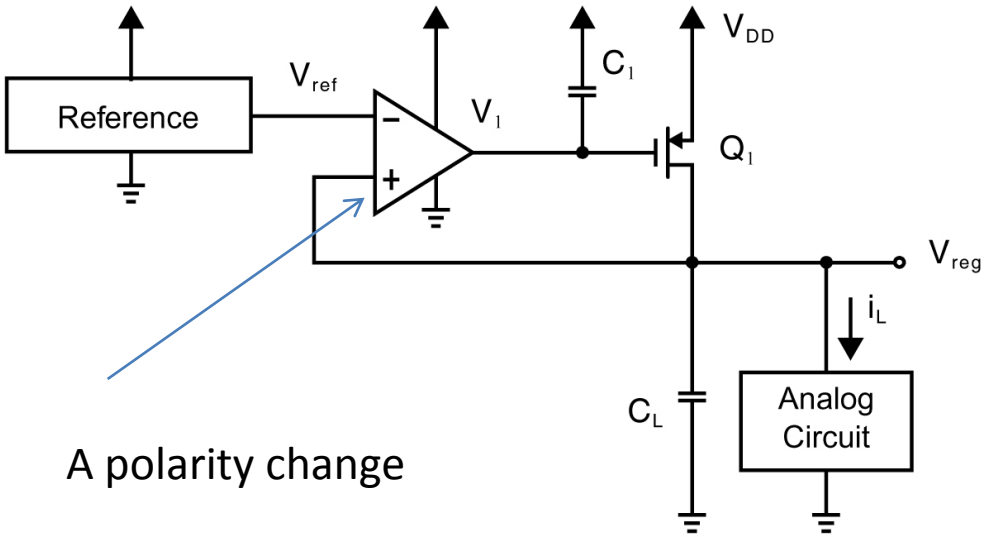
Generally, ω_z will be at a much higher frequency than the poles and have little effect on stability.

7.4.3 Low dropout regulators

When the regulated output must be at a voltage only 200–400 mV below V_{DD}, and especially when native (near-zero-V_t) NMOS devices are unavailable, it is necessary to utilize a PMOS device for Q_1 as shown in Fig. 7.19. In this case, the gate voltage V_1 is well below V_{DD} so the dropout voltage is only limited by $V_{eff,1}$. This is commonly referred to as a *low dropout (LDO) voltage regulator* and is popular when power efficiency is critical.

Although the resistance seen looking into Q_1 is increased the loop gain is also increased so the regulator's closed-loop output resistance is roughly the same.

A significant drawback of PMOS devices is their reduced power supply rejection. With respect to small signals at V_{DD}, Q_1 behaves like a common-gate amplifier having considerable gain.



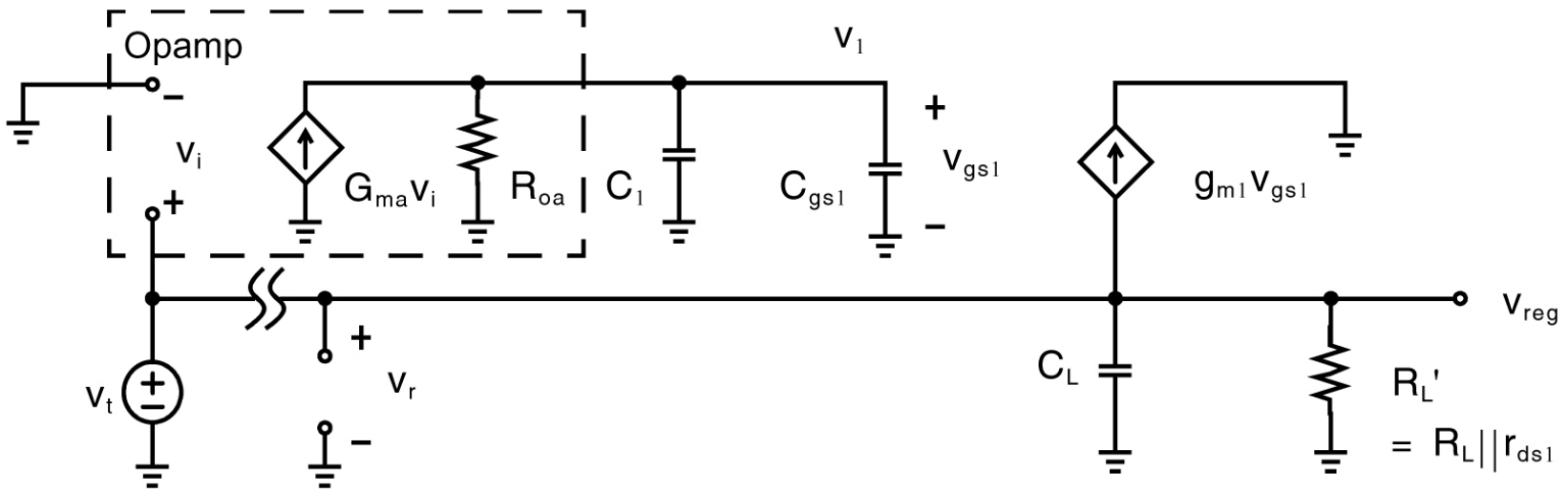
Chapter 7 Figure 19

Neglecting C_{gd} of the transistor $$L(s) = \frac{G_{ma}R_{oa}g_{m1}R_L'}{\left(1+\frac{s}{\omega_{pa}}\right)\left(1+\frac{s}{\omega_{pL}}\right)}$$

The pole at the amplifier output (gate of Q_1) is $\omega_{pa} = \frac{1}{R_{oa}C_1'}$ where $C_1' = C_1 + C_{gs1}$

and the output pole is $\omega_{pL} = \frac{1}{R_L'C_L}$

Again, either pole can be made dominant to compensate the loop.

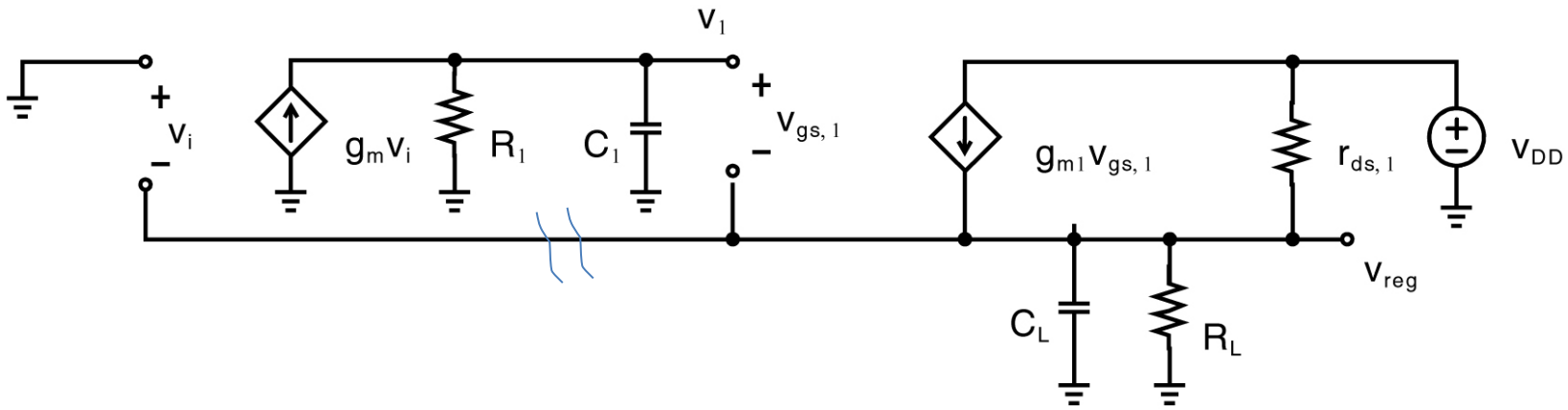


Chapter 7 Figure 20

PSRR

Open loop $A(s) = V_{reg}(s)/V_{DD}(s)$

Then closed loop $A_f(s) = A(s)/[1+L(s)] = PSRR^{-1}$



Chapter 7 Figure 21