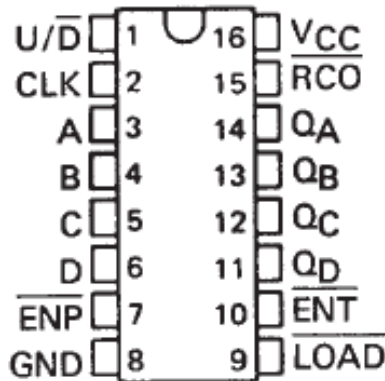


# 74LS168

## SYNCHRONOUS 4-BIT BCD UP/DOWN COUNTER



The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ( $\overline{\text{ENP}}$ ,  $\overline{\text{ENT}}$ ) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input ENT is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the  $Q_A$  output when counting up and approximately equal to the low portion of the  $Q_A$  output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the  $\overline{\text{ENP}}$  or  $\overline{\text{ENT}}$  inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

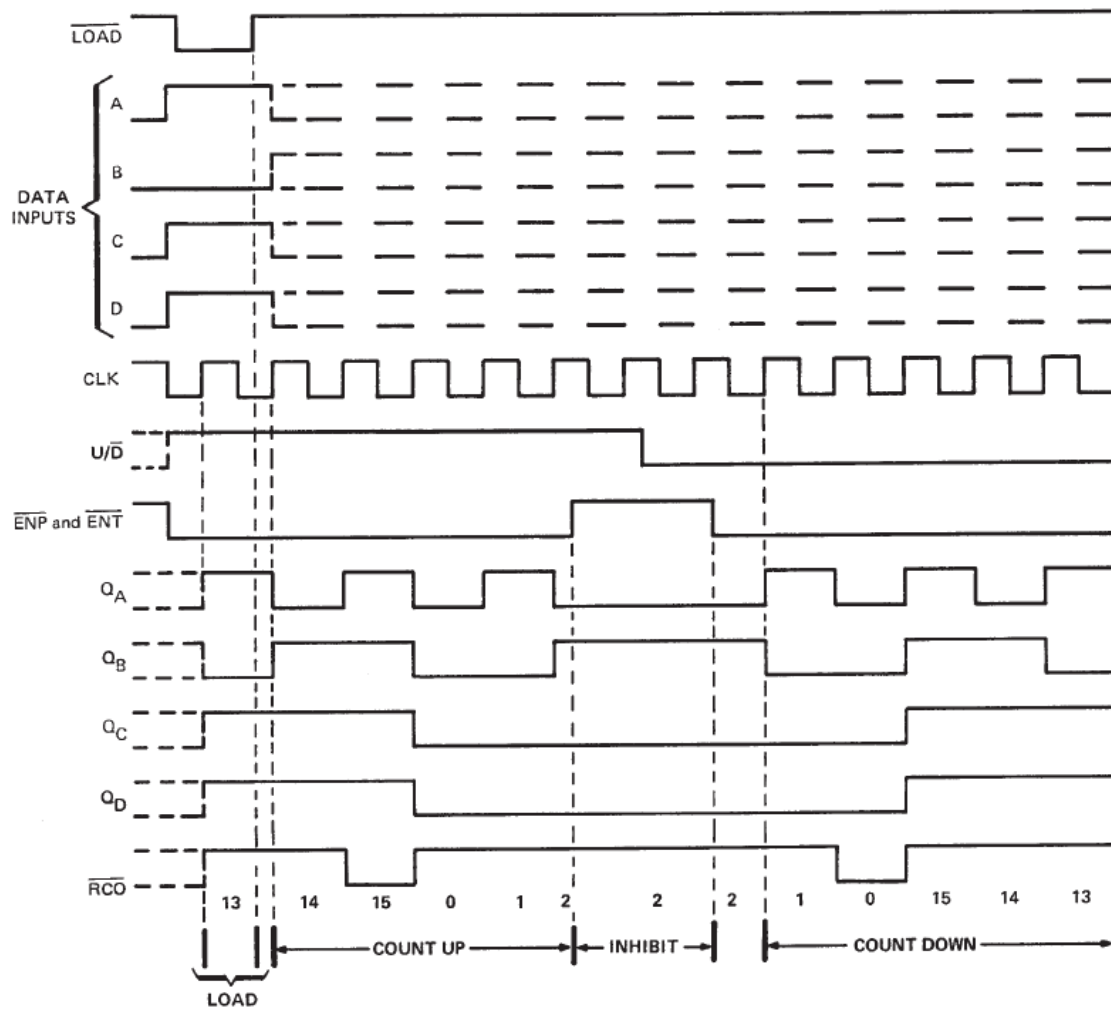
These counters feature a fully independent clock circuit. Changes at control inputs ( $\overline{\text{ENP}}$ ,  $\overline{\text{ENT}}$ ,  $\overline{\text{LOAD}}$ , U/D) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

## Timing Diagram

### typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



Source: Texas Instruments TTL Data Book