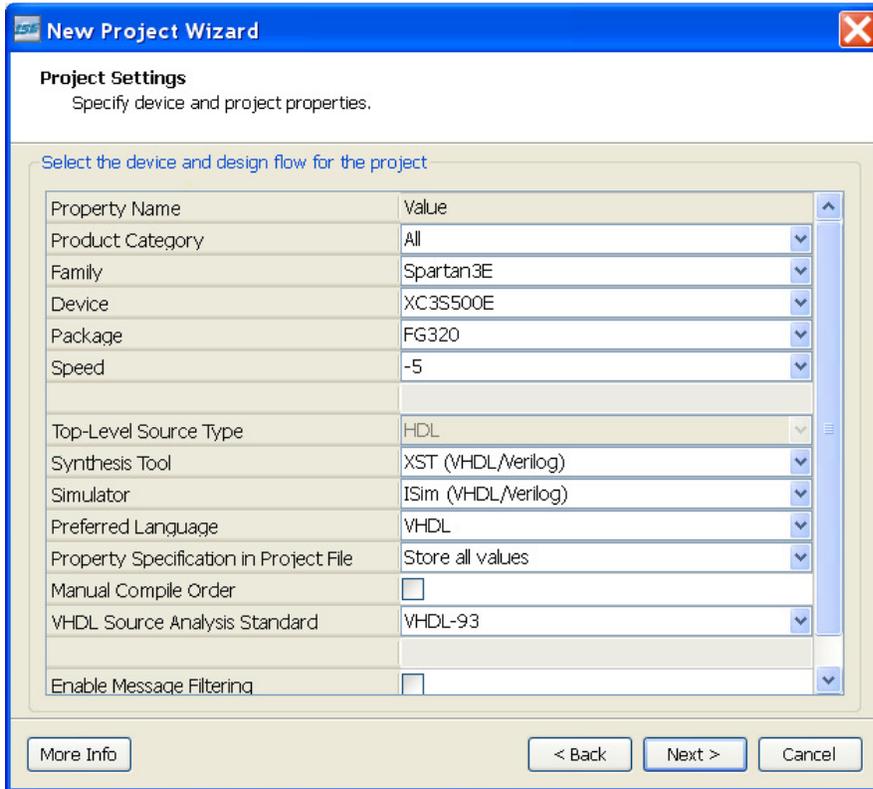


Device and Design Flow Setup

Family: Spartan3E

Device: XC3S500E or XC3S1200E depending on the board

Package: FG320



The screenshot shows the 'New Project Wizard' dialog box with the 'Project Settings' tab selected. The dialog is titled 'New Project Wizard' and has a close button in the top right corner. Below the title bar, the text 'Project Settings' is followed by the instruction 'Specify device and project properties.' A section titled 'Select the device and design flow for the project' contains a table of settings. The table has two columns: 'Property Name' and 'Value'. The settings are as follows:

Property Name	Value
Product Category	All
Family	Spartan3E
Device	XC3S500E
Package	FG320
Speed	-5
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

At the bottom of the dialog, there are three buttons: 'More Info', '< Back', and 'Next >', and a 'Cancel' button on the far right.

The above example was created for the XC3S500E chip which has 500K gates. If the FPGA chip on your board is XC3S1200E (1200K gate version), you must set the device to XC3S1200E.