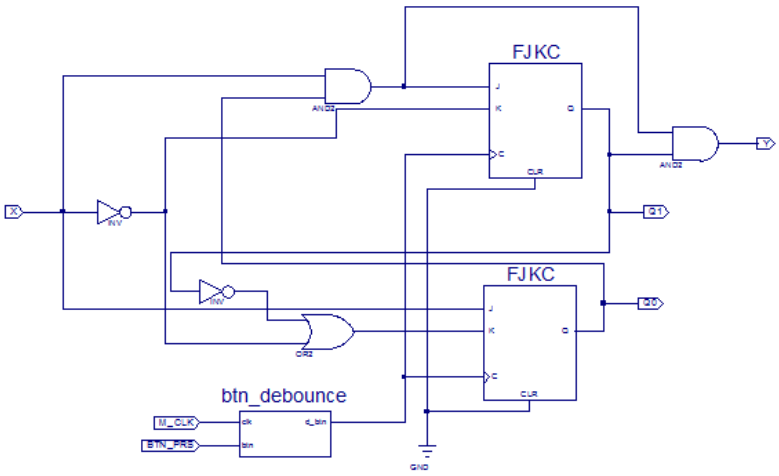
EE 1315 DIGITAL LOGIC LAB
EE Dept, UMD

EXPERIMENT # 9: Analysis of Synchronous Sequential Circuit

The circuit given below has one input x and one output y. Due to the internal sequential states created by FFs, the output not only depends on the current input but also on the history of it. We wish to analyze this behavior and determine its functionality.



This experiment works as follows. First, theoretically analyze the given circuit without actually building it. Next, build the circuit, and verify whether your theoretical analysis matches with the actual output. The result section follows these two steps. Remember to **right click** on the project in the **design** tab and choose **add module**. Navigate to **C:\Xilinx\debounce\debounce.vhd** and select **Open**. A window should appear that indicates the successful addition of the module to your project. Click **OK**.

For JK-ffs, you should use the fjkc available in the Flip_Flop category of the Xilinx ISE library. In the second part of this lab, use the following Scalar Port assignments to determine the operation of the circuit. The Q1 and Q0 outputs are not necessary for this lab, but will help you to visualize state changes that are occurring and aid in debugging the circuit if you have difficulty.

	Inputs			Outputs		
Scalar Port	**X**	**M_CLK**	**BTN_PRS**	**Y**	**Q0**	**Q1**
Site	**G18**	**B8**	**B18**	**J14**	**E17**	**P15**

EXPERIMENT #9 RESULTS

(Print the following pages and bring them with you to the lab session)

Your Name: _____

Witnessed by Instructor or TA: _____

Date _____

Show your design process.

Step 1) Derive FF next state and output equations

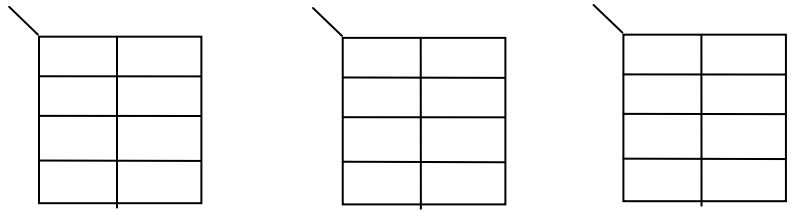
$A(t+1) = J_1Q' + K_1'Q =$_____

$B(t+1) = J_2Q' + K_2'Q =$_____

y = _____

Step 2) Derive the state table

A(t+1) B(t+1) y



State Table Using Binary Bits

PS	NS

State Table Using Letter Symbols

PS	NS

Step 3) Draw the state diagram

Step 4) Create a sample input sequence and find the corresponding output sequence (i.e. the circuit's functionality)

Step 5) Build the circuit using Xilinx ISE.

Step 6) Verify your input/output sequence by testing the completed circuit on the FPGA.

Record your run results and show to your TA.