Default Part and Product Family Setup

Board: Nexys4 DDR FPGA Family: Artix 7 Part number: xc7a100tcsg324-1 Package: CSG324 Preferred Language: VHDL VHDL Source Analysis Standard: VHDL-93

À New Project	×
	New Project Summary
HLx Editions	A new RTL project named 'lab1_or' will be created.
	The default part and product family for the new project: Default Board: Nexys4 DDR Default Part: xc7a100tcsg324-1 Product: Artix-7 Family: Artix-7 Package: csg324 Speed Grade: -1
£ XILINX.	To create the project, click Finish
?	< <u>B</u> ack <u>N</u> ext > <u>Finish</u> Cancel